

MS-7680

Ver:3.1

m-ATX : 245 X 210mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71889AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UP1625 4+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT CPU SA

Controller:uP6103

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x8

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

LPT Header *1

on BOARD BUZZER

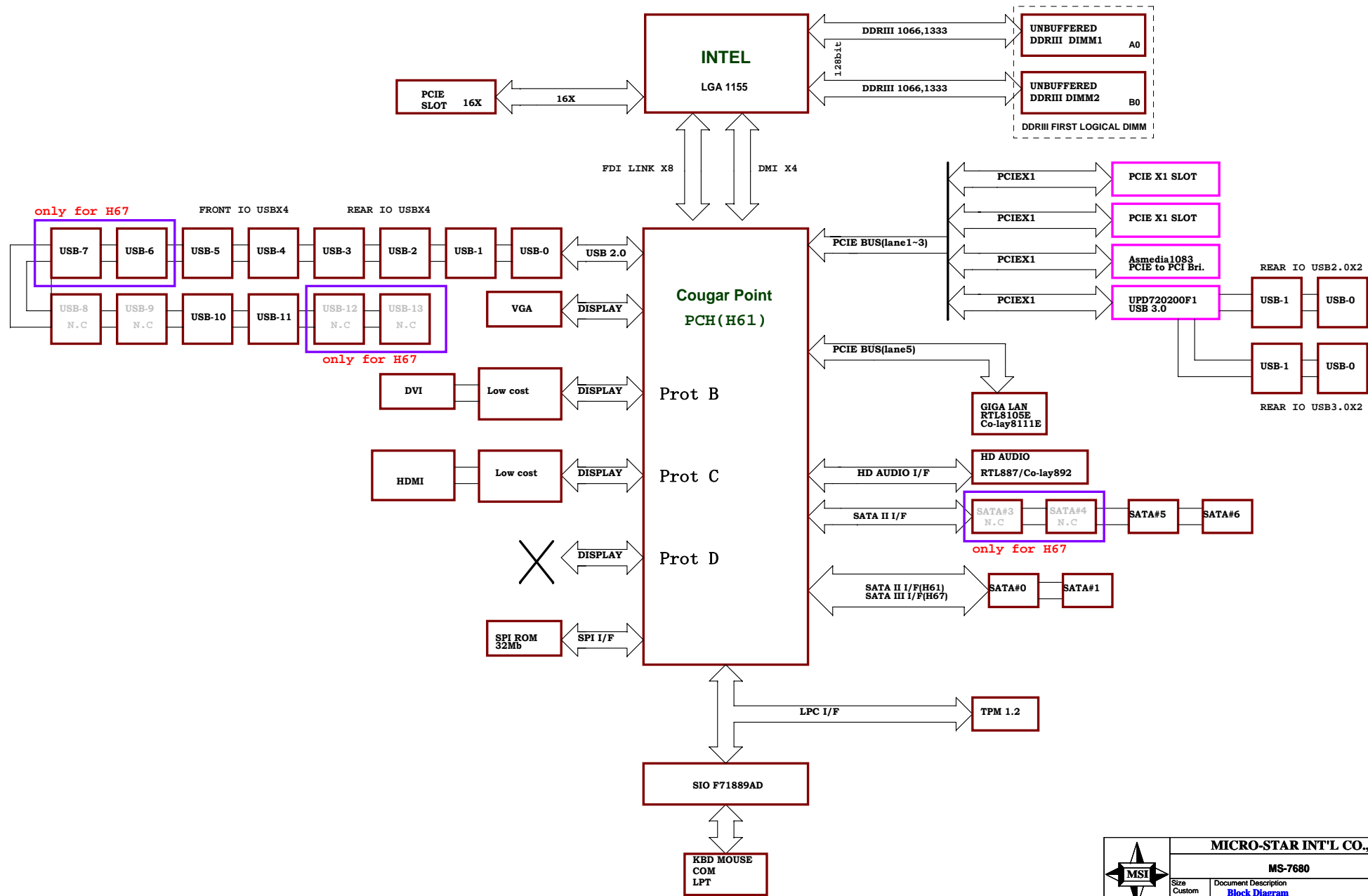
Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG	3
CPU-Memory	4
CPU-Power	5
CPU-GND	6
DDR III DIMM 1	7
DDR III DIMM 2	8
CP-PCI/E/DMI/USB/CLK	9
CP-SATA/HOST/FAN/GPIO/VGA	10
CP-SMB/LPC/AUDIO/RTC	11
CP-POWER	12
CP-GND/NVRAM	13
CP Strap	14
PCIEx16 /x1 /x1HDA CO-LAY	15
PCIEx1 Slots	16
SIO-Fintek F71889AD(EUP)	17
LAN - RTL8111E	18
ALC887VD_COLAY_ALC892	19
DVI transfer	20
HDMI	21
VGA	22
SATA / FAN Control	23
USB Connector	24
ACPI Controller UPI	25
Power Saving circuit&APS	26
DDR Power - uP6103 1-Phase	27
PCH Power - uP6103 1-Phase	28
CPU_VTT - uP6103- 1-Phase	29
CPU_SA - uP6103 1-Phase	30
VRD12 - uPI6234	31
uPI6234 3-Phase CPU	32
uPI6234 1-Phase GPU	33
ATX F_Panel/EMI/TPM/LPT	34
XDP / Manual Parts	35

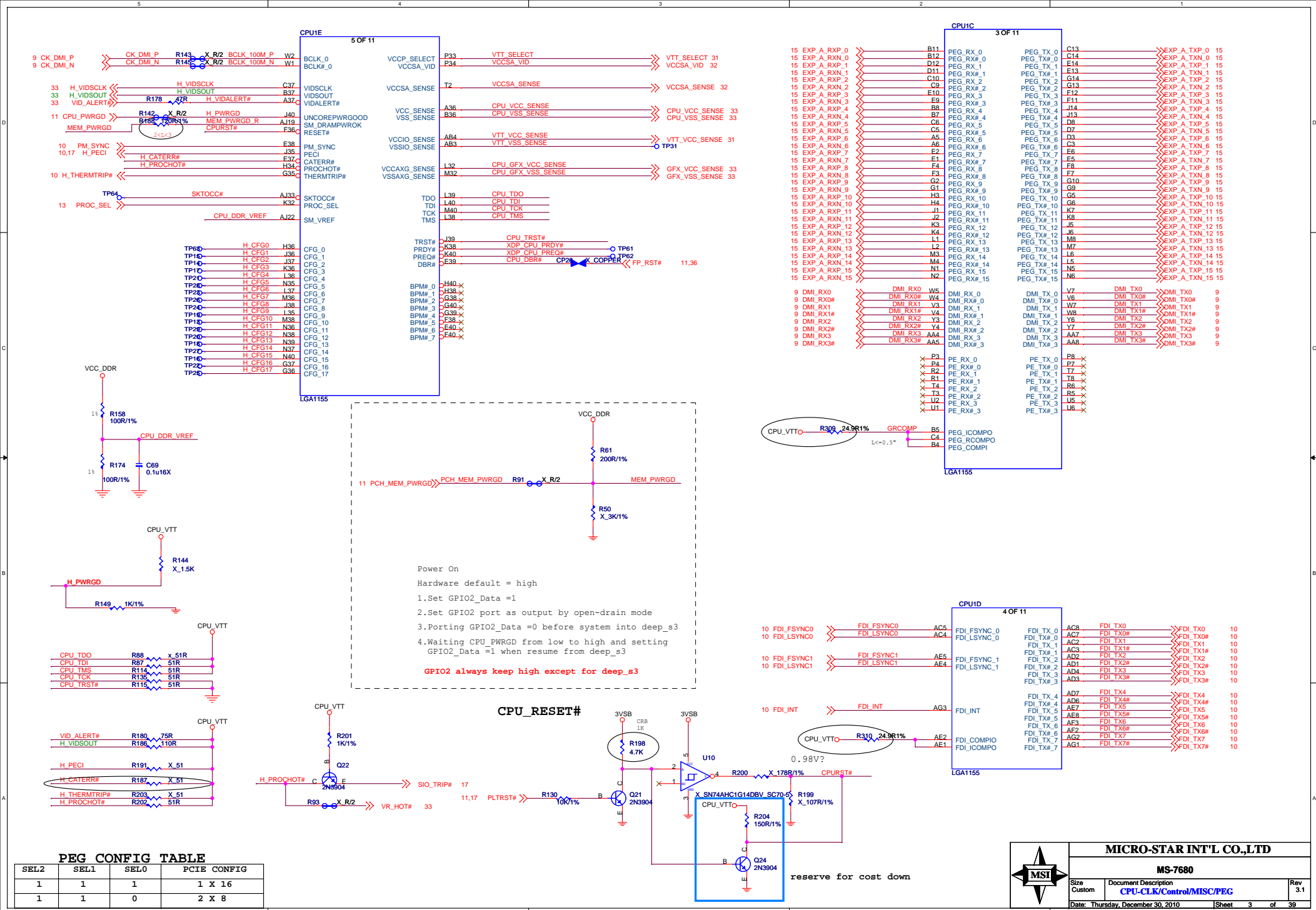


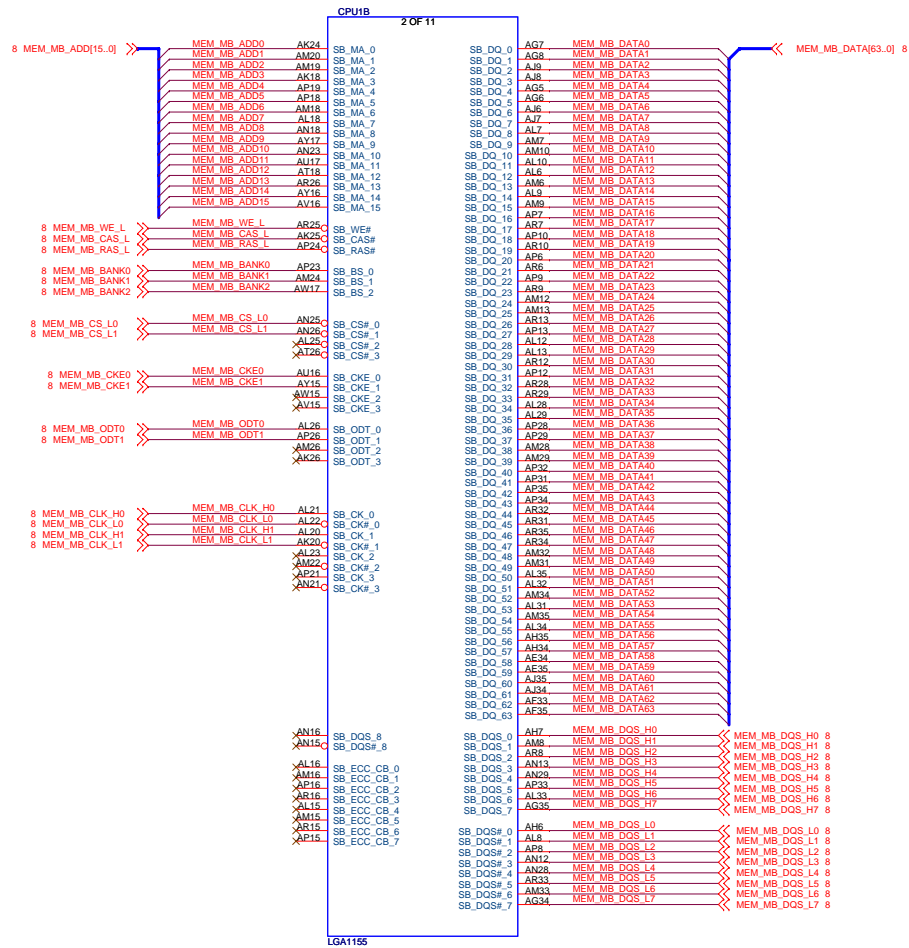
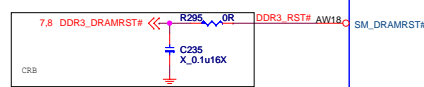
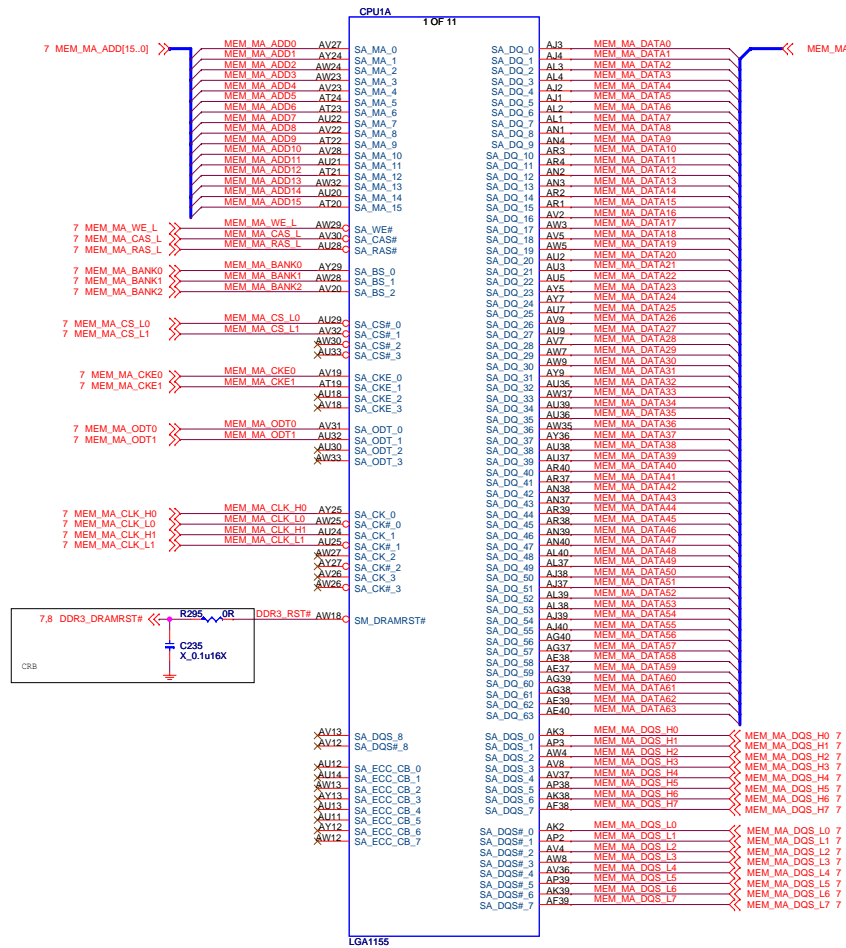
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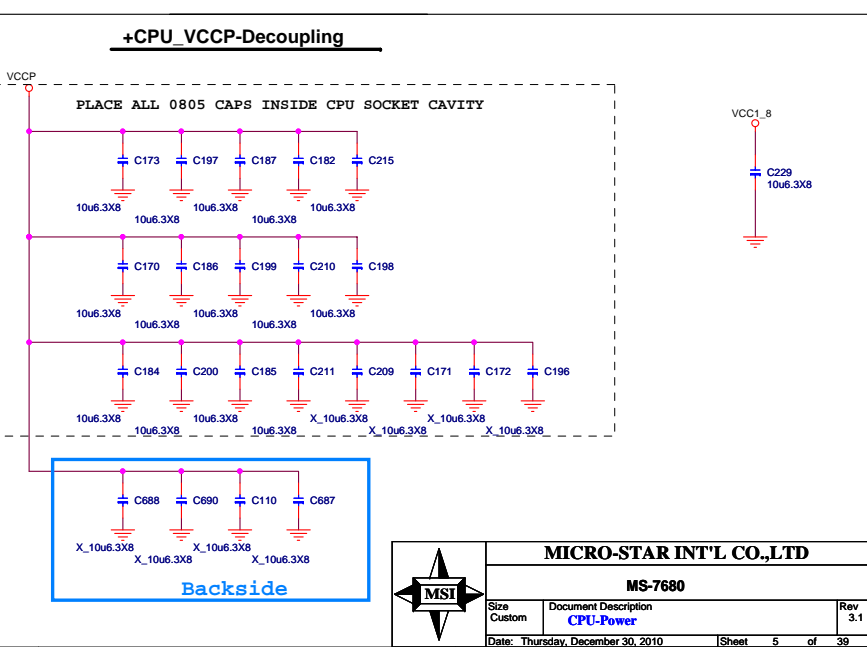
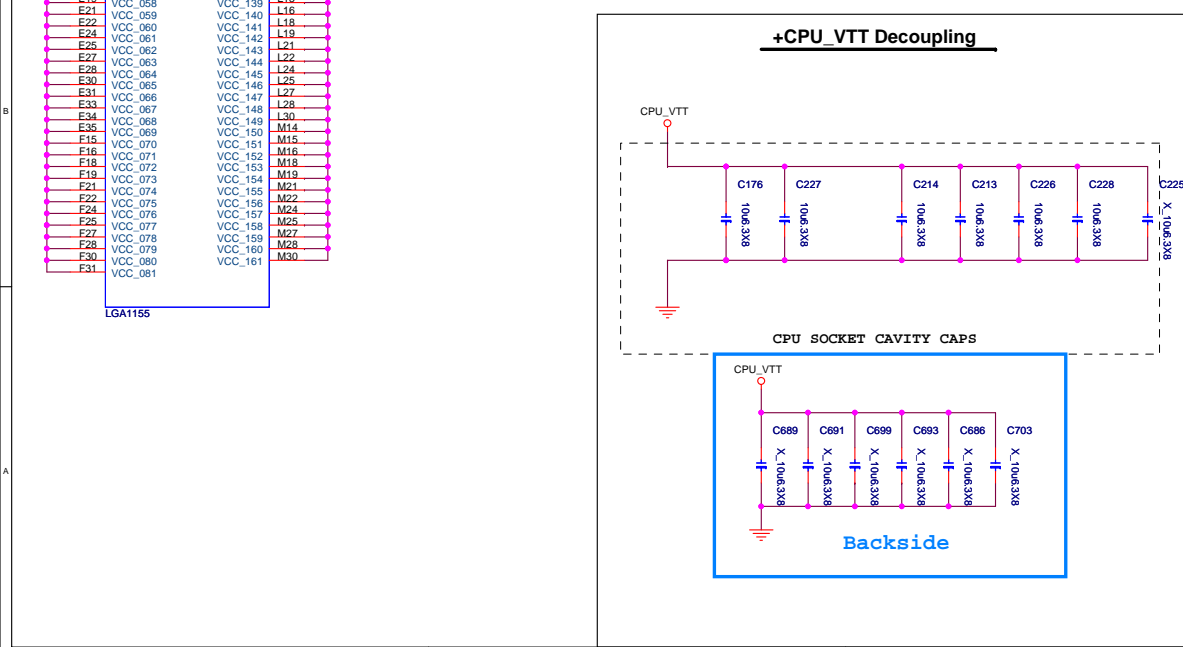
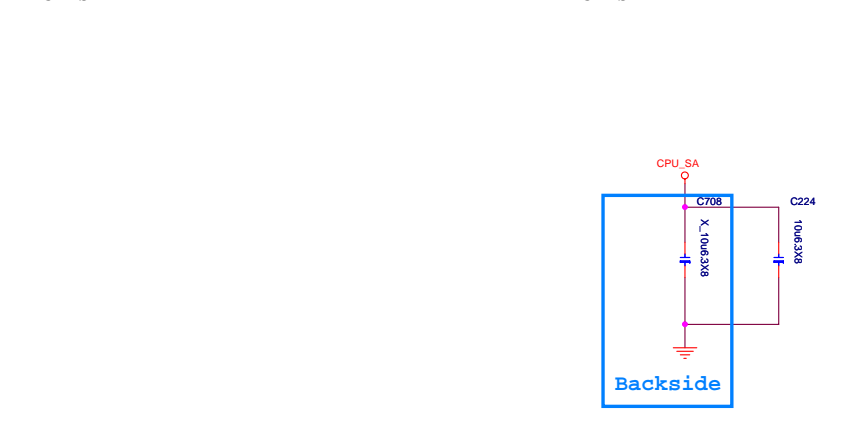
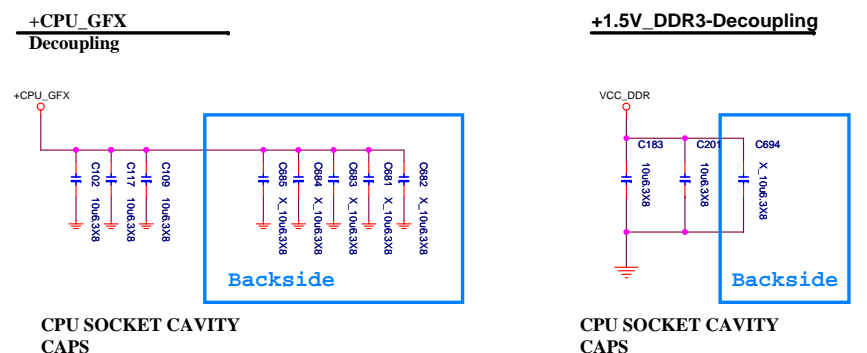
MS-7680

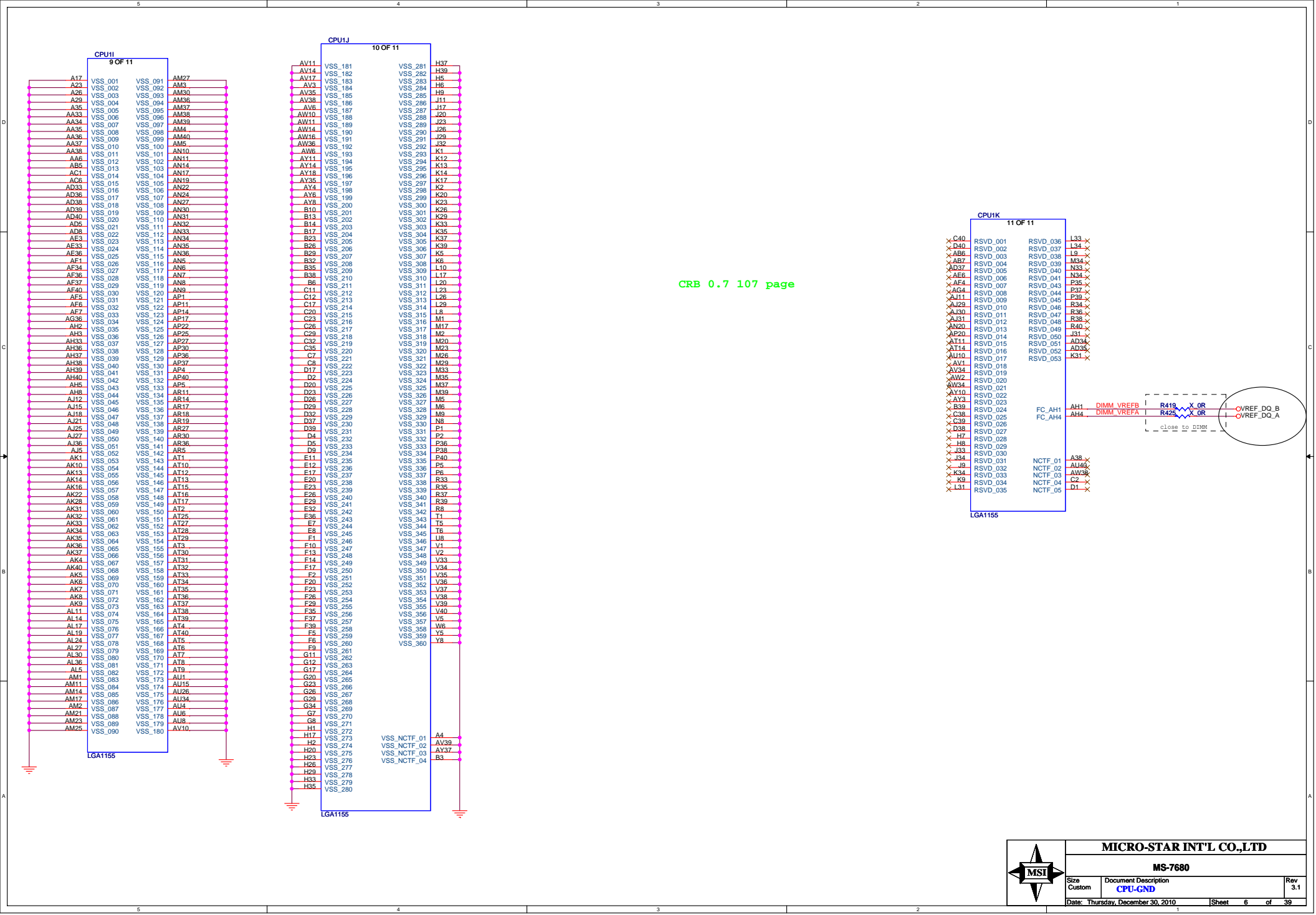
Size	Document Description	Rev
Custom	Cover Sheet	3.1
Date: Friday, December 17, 2010 Sheet 1 of 39		







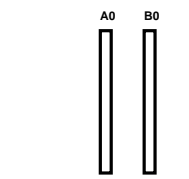




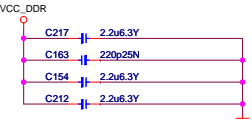
DDR3 DIMM_A0

DDR3 DIMM_A1

4 MEM_MA_DATA[63:0] MEM_MA_DATA[63:0]



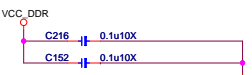
Place close to DIMM1



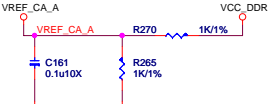
Place close to DIMM1 with DIMM2



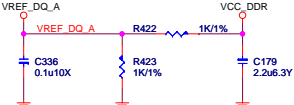
Place close to DIMM2



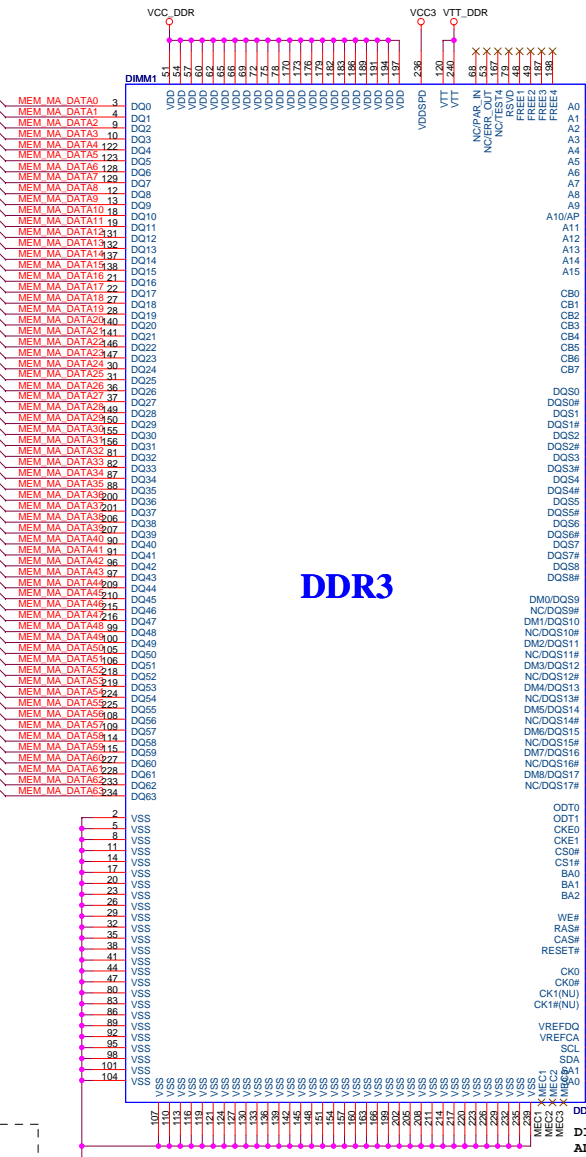
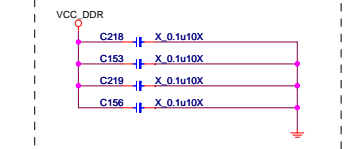
UPI VOLTAGE CONSOLE



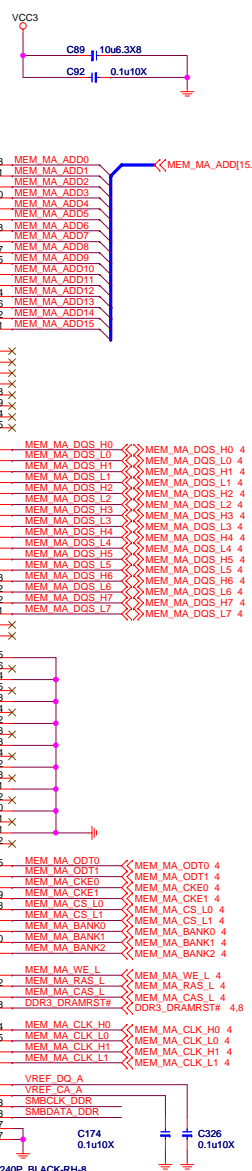
UPI VOLTAGE CONSOLE



EMI



uP6262 use BMA8
PN: I34-6262B09-U33



DDR3-240P_BLACK-RH-8
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

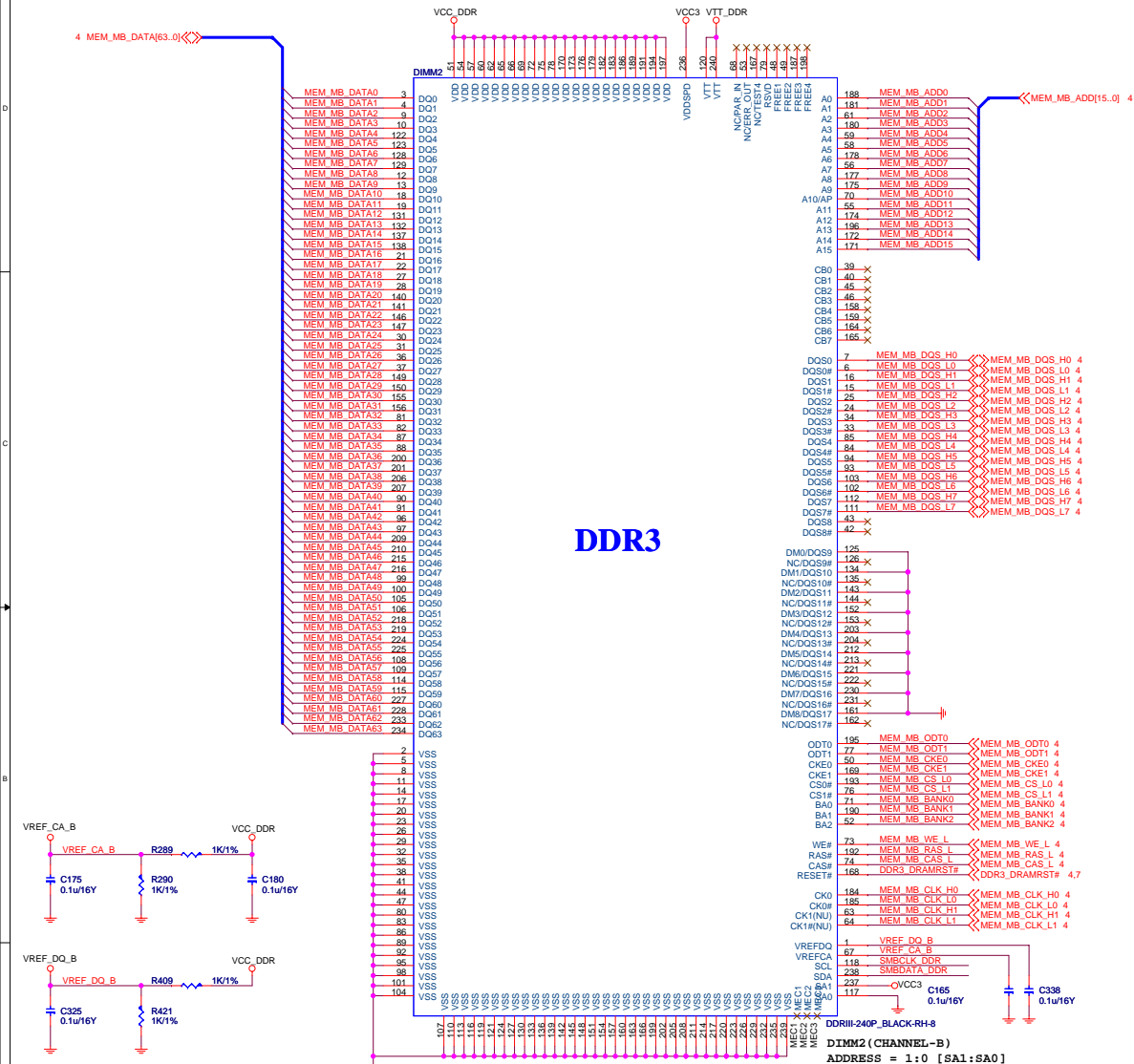
VCC3 C89 10u6.3X8 C92 0.1u10X

8 SMBCLK_DDR SMBCLK_DDR R159 33R SMBCLK 11,15,16,29
8 SMBDATA_DDR SMBDATA_D0R173 33R SMBDATA 11,15,16,29



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MS-7680			
Size	Document Description	Rev	
Custom	DDR III DIMM 1 / DIMM 2	3.1	
Date: Thursday, December 30, 2010		Sheet	7 of 39

DDRIII DIMM_B0



SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7



MICRO-STAR INT'L CO.,LTD

MS-7680

Size Custom	Document Description DDR III DIMM 3 / DIMM 4	Rev 3.1
Date: Thursday, December 30, 2010		Sheet 8 of 39

REQUIRED STRAPS

Internal pull-up
Internal pull-up

BM_BUSY# R529 10K/1%
LPC_DRQ#0 R714 X 10K
LPC_DRQ#1 R702 X 10K
STP_PCH# R622 10K/1%
SMBCLK R668 1.8K
SMBDATA R667 1.8K
FP_RST# R562 10K/1%
PCH_GPIO35 R624 X 10K

FP_RST# R564 X 10K/1%
SIO_PME# R703 10K/1%
SPI_HOLD_GPO# R641 X 8.2K

S_LP_LAN# R647 X 10K/1%
PCH_GPIO24 R647 X 220K
PCH_GPIO28 R623 X 10K/1%
PCH_GPIO72 R538 10K/1%
SB_WAKE# R636 1K
R/# R655 10K/1%
SMLINK0_CLK R665 10K/1%
SMLINK0_DATA R666 10K/1%
PCH_SML0ALERT# R660 10K/1%
PCH_SMLTCLK R659 10K/1%
PCH_SML1DATA R674 10K/1%
PCH_SML1ALERT# R669 10K/1%
USB3_SMI# R683 10K/1%

CRB pull down
PCH_GPIO57 R690 10K/1%
R669 X 10K/1%

SUSWRN# CP R682 X OR
RSMRST# R806 X OR

PCH_GPIO31 R675 10K/1%
PCH_GPIO27 R762 10K/1%
SUSACK# CP R16 10K
DPWROK_CP R25 10K

PCIECLKREQ0# R574 10K/1%
PCIECLKREQ5# R634 10K/1%
PCIECLKREQ6# R538 10K/1%
PCIECLKREQ7# R640 10K/1%
PCH_GPIO33 R717 X 1K

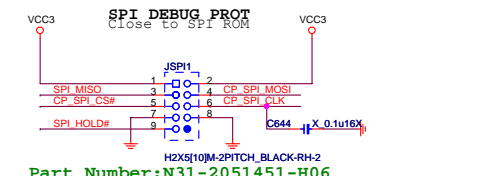
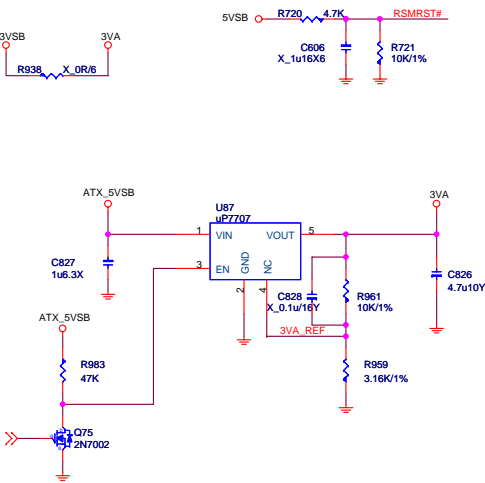
PCIECLKREQ can't find 0/1/3/4

SUSWRN# CP R700 X 10K/1%
R665 X 10K/1%

3VA

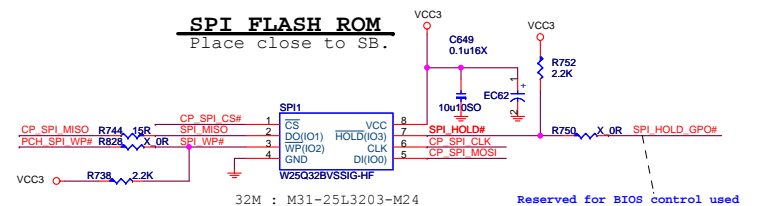
20mA

17 CP_3VA_OFF



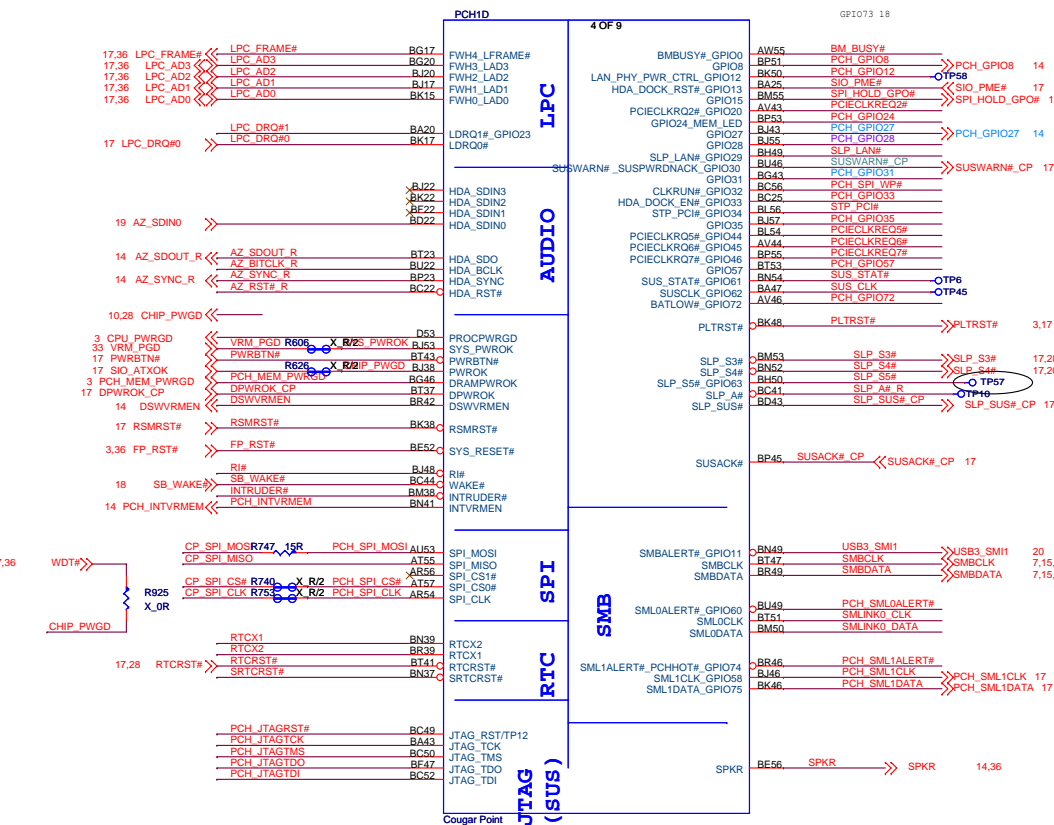
SPI FLASH ROM

Place close to SB.



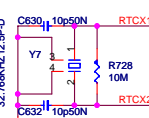
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MS-7680			
Size	Document Description	Rev	
Custom	CP-SMB/LPC/AUDIO/RTC	3.1	
Date: Tuesday, January 04, 2011	Sheet	11	of 39

Reserved for BIOS control used

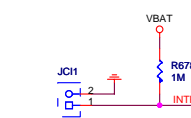


RTC Block

Close to PCH



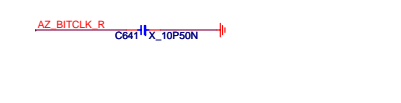
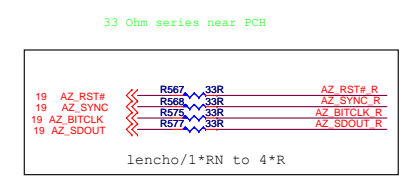
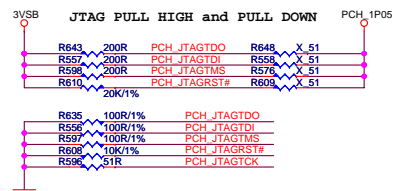
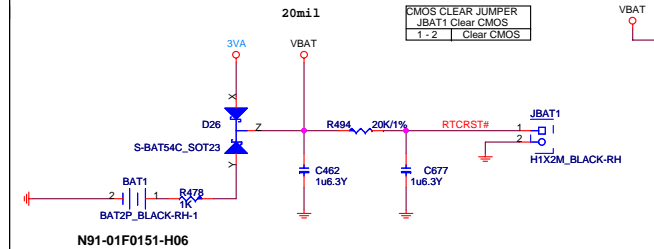
Chassis Intrusion



RTC and CLR_CMOS

Clear CMOS

CMOS CLEAR JUMPER	
JBAT1 Clear CMOS	1 - 2 Clear CMOS



Change to 100H if
VCCA_DPLL1/VCCA_DPLL2
has noise issue.

PCH_1P05

R460 X_0.8

VCCA_FDIPLL

C415 10u6.3X8

R526 X_0R

VCCA_CLK

NO THIS PIN

R461 X_0.8

VCCA_PLDM12

C417 10u6.3X8

C426 1u6.3X

CP25 X COPPER

VCCA_CKDMI

C550 10u6.3X8

C551 1u6.3X

CP22 X COPPER

VCCA_DPLL1

to b

EC46 X_100u16SO

C460 22u6.3X8

C472 1u6.3X

CP22 X COPPER

VCCA_DPLL2

EC47 X_100u16SO

C474 22u6.3X8

C475 1u6.3X

PCH_1P05

L23

DMI PLL FILTER

X_L10U_500mA_0805

VCCA_PLEX

C420 X_10u6.3X8

C427 1u6.3X

L24

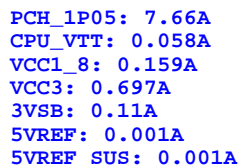
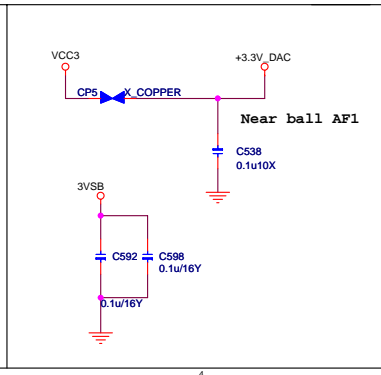
SATA PLL FILTER

X_L10U_100mA_0805

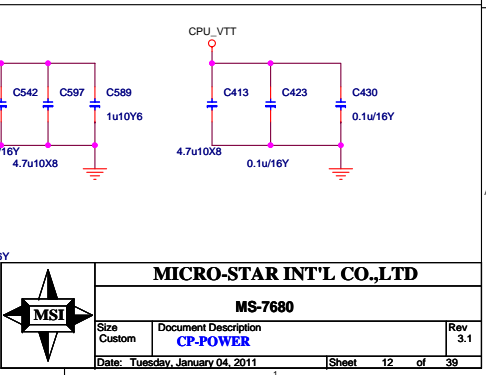
VCCA_PLSATA

C459 X_10u6.3X8

C464 1u6.3X

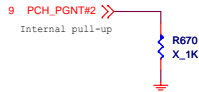
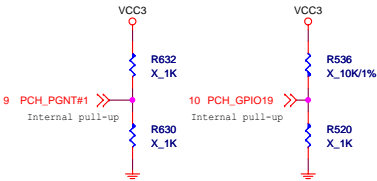
[illegible]

PCH decoupling cap

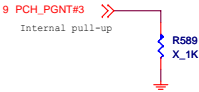


PCH Straps

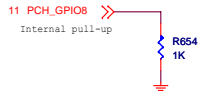
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



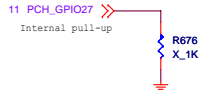
DMI AC/DC MODE
0 : AC
1 : DC *



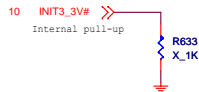
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM) *
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????????
1 : ?????????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



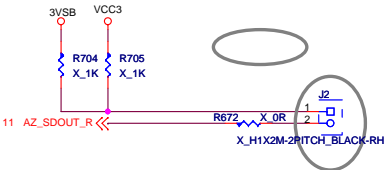
INTRVREM
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the
integrated GbE only operates at 10/100 Mbps during S3-S5.



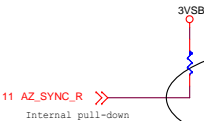
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V
regulators. Must beconnected even when not supporting DSW.



HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

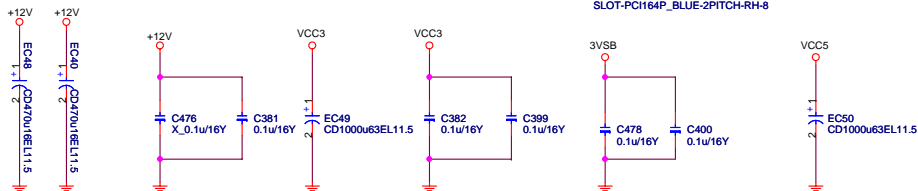
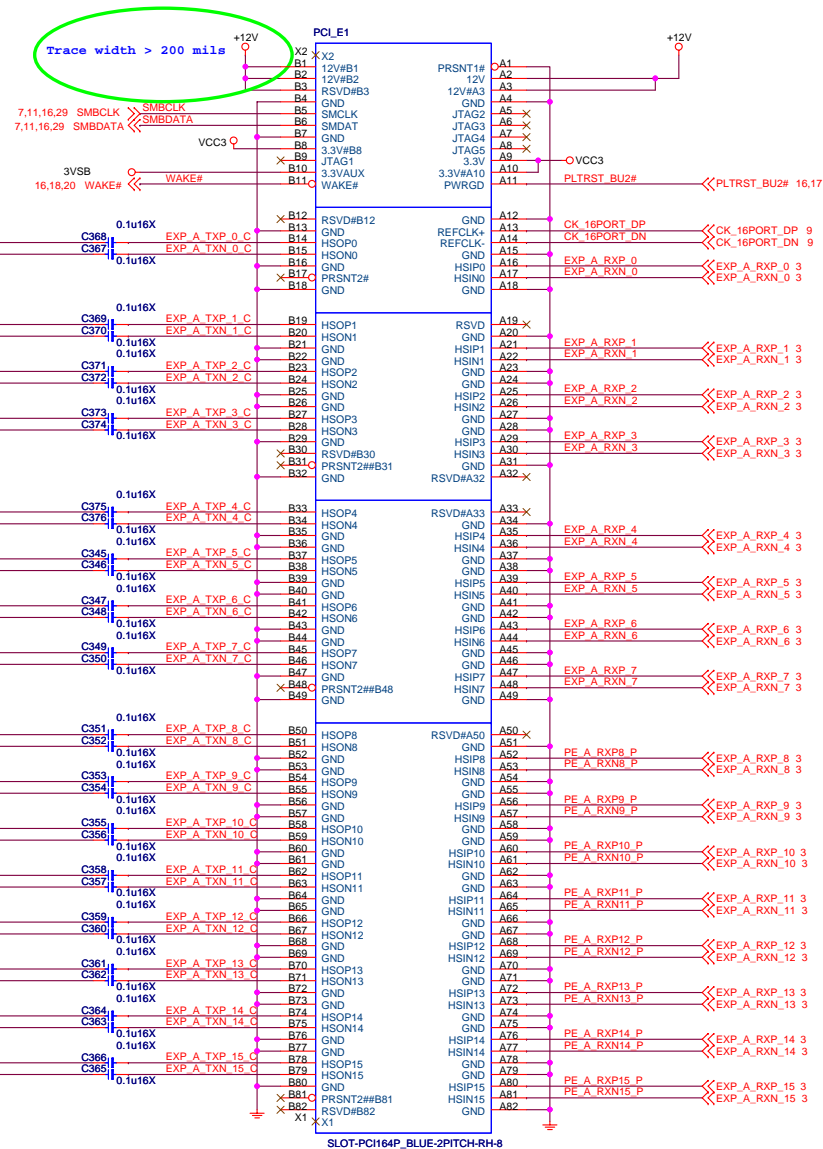


DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC I.SF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

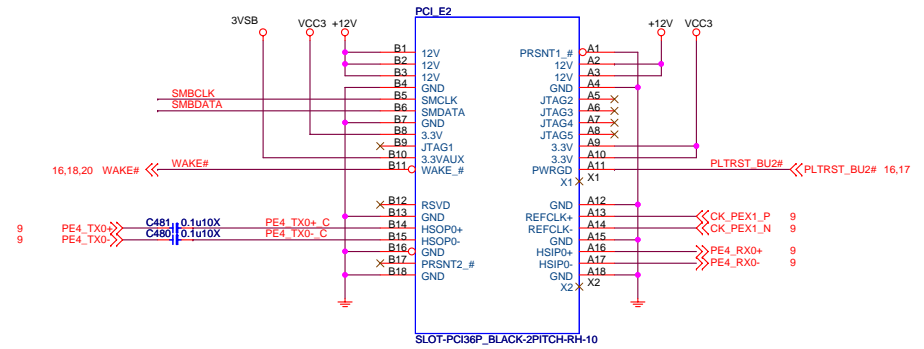


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

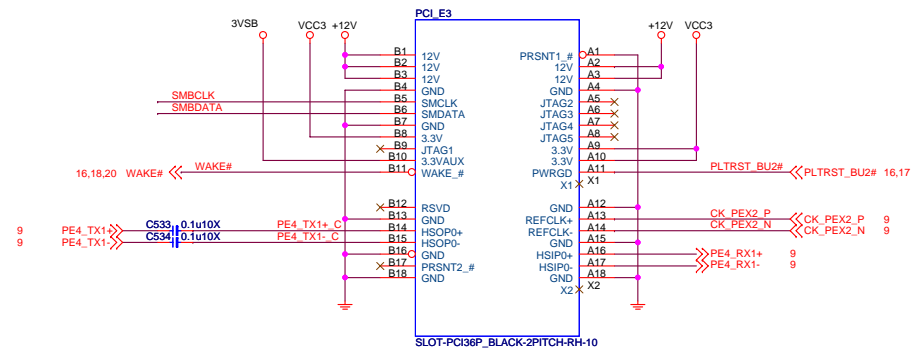
PCI_Express X16 Slot



PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT

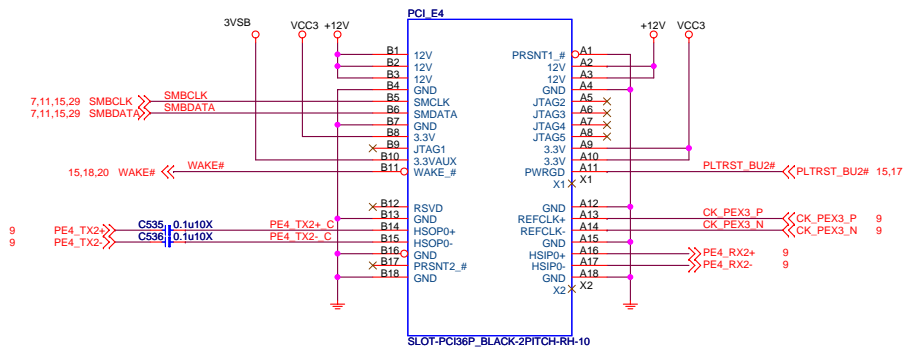


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MS-7680

Size Custom	Document Description PCIE x16 /x1/x1	Rev 3.1
Date: Thursday, December 30, 2010		Sheet 15 of 39

PCI EXPRESS x1-PORT



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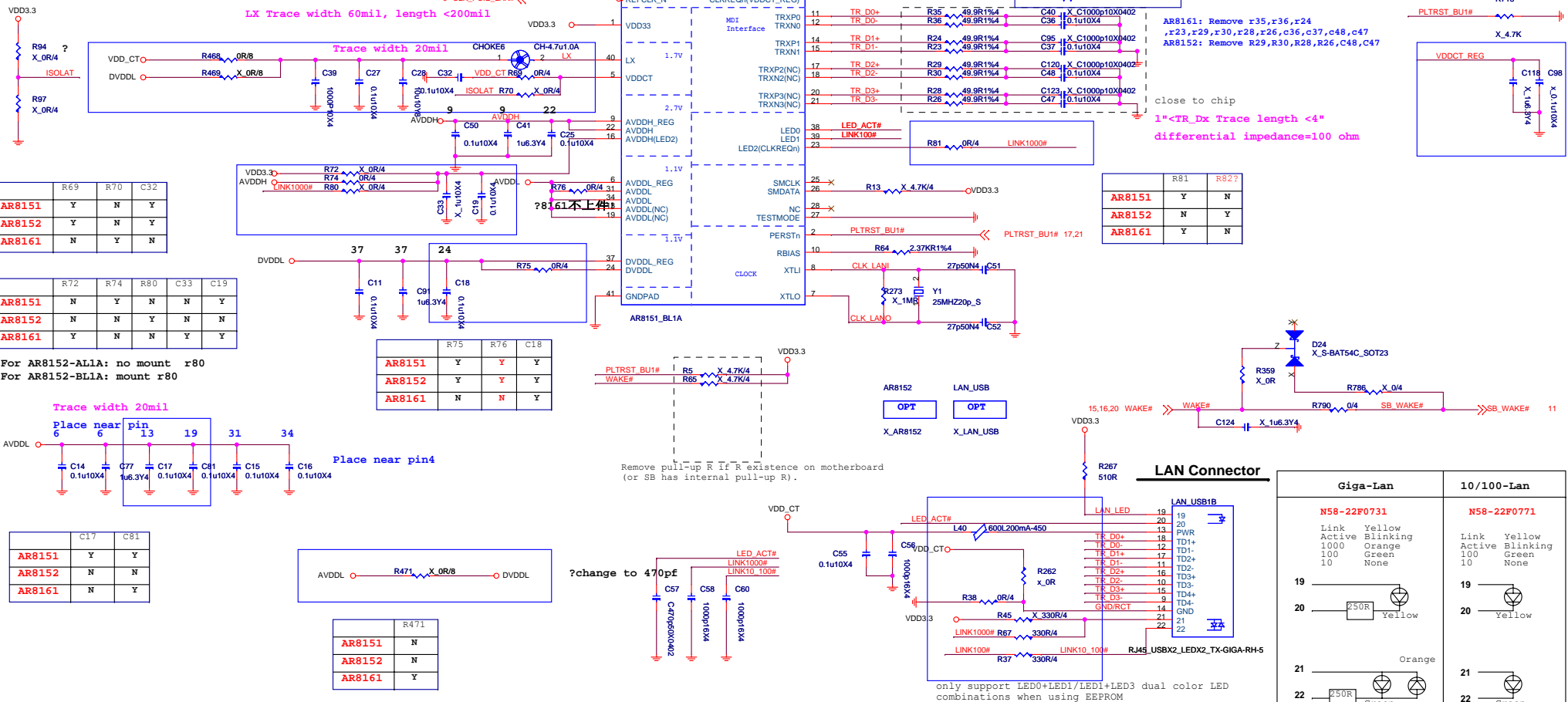
MS-7680

Size	Document Description	Rev
Custom	PCIE x16 /x1/x1	3.1
Date:	Thursday, December 30, 2010	Sheet 16 of 39

2				
	R89	R86?	C118	C98
AR8151	N	Y	N	N
AR8152	N	N	N	N
AR8161	N	Y	N	N

Trace width >40mil

	R471
AR8151	N
AR8152	N
AR8161	Y

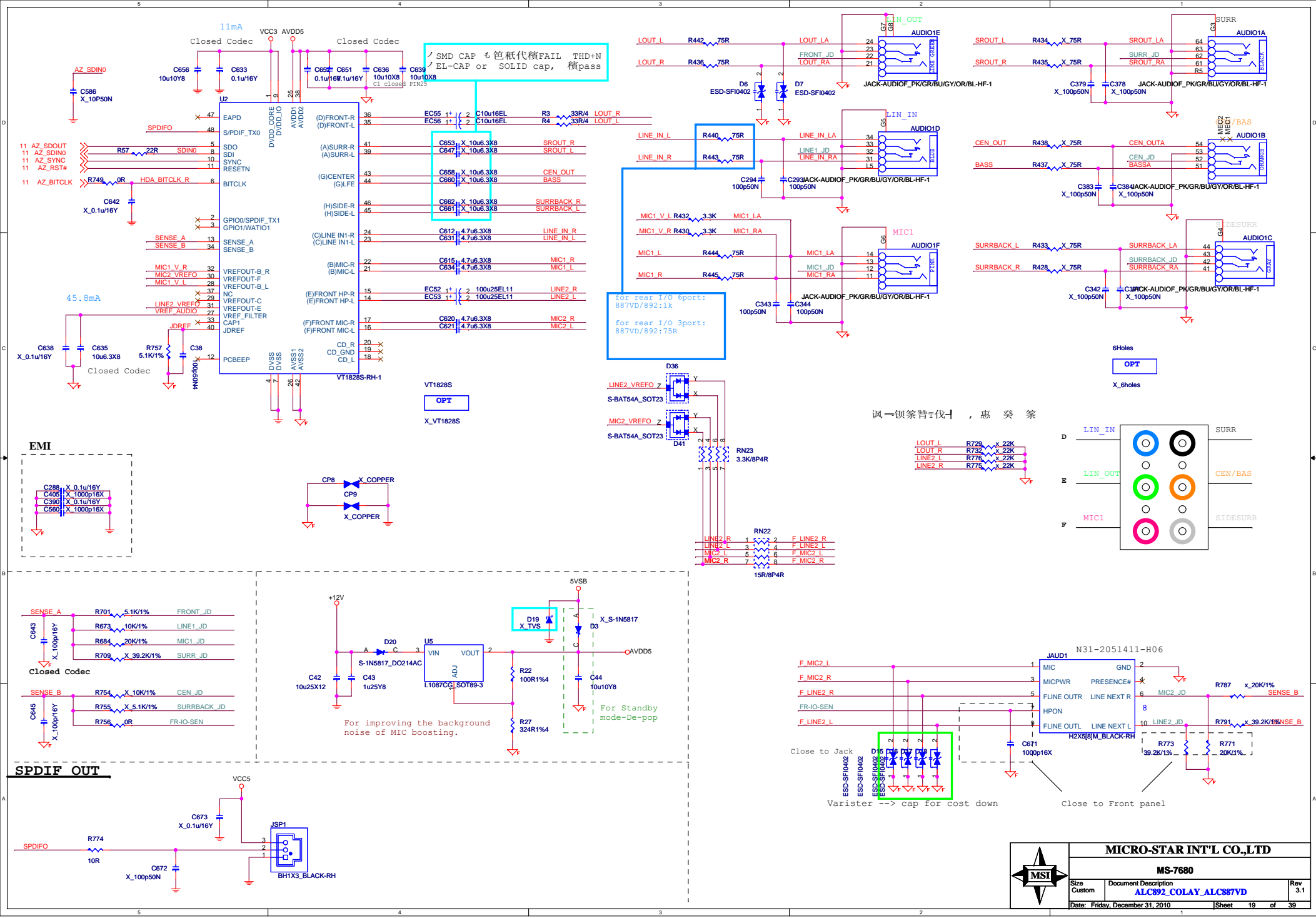


	R262	R38	R45	R67
AR8151	N	Y	N	Y
AR8152	Y	N	Y	N
AR8161	N	Y	N	Y

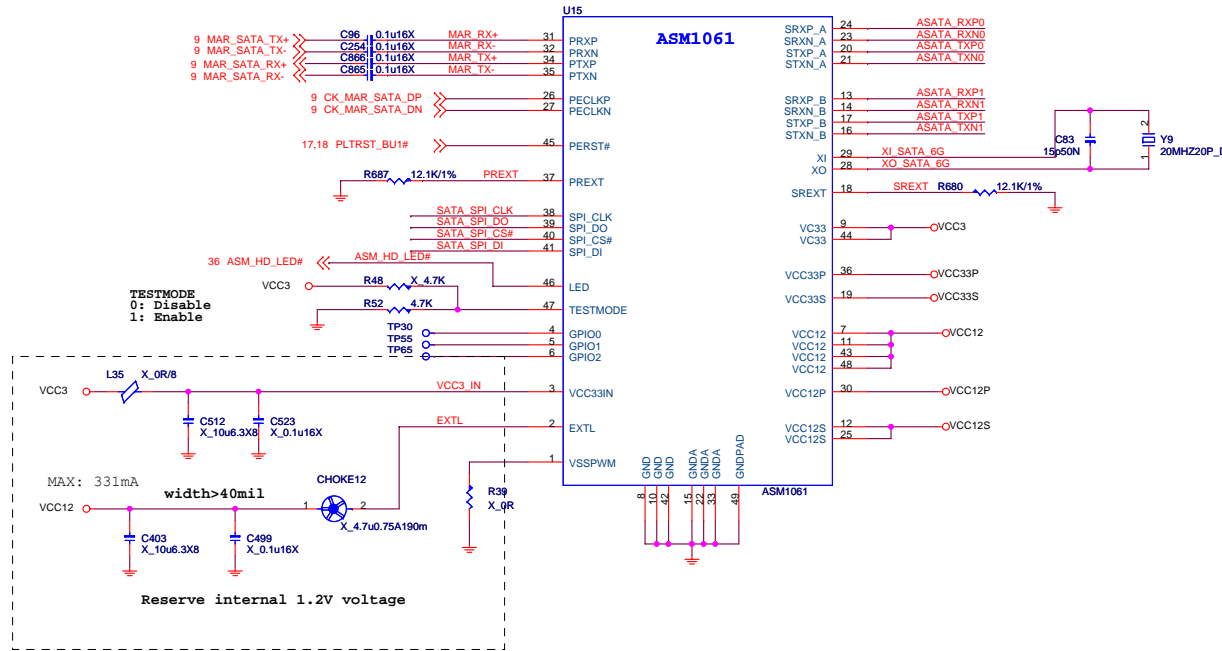


MS-7680

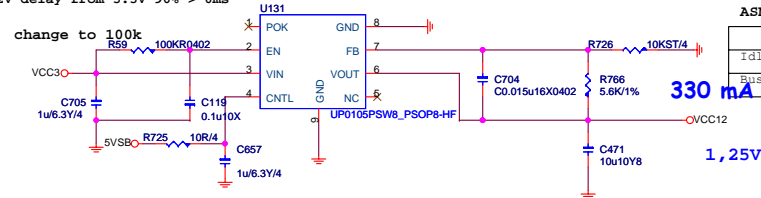
Size Custom	Document Description LAN - RTL8111E / 8105E	Rev 3.1
Date: Tuesday, January 04, 2011		Sheet 18 of 39



ASM1061 SATA6G



1.2V delay from 3.3V 90% > 0ms

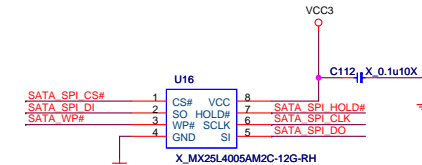
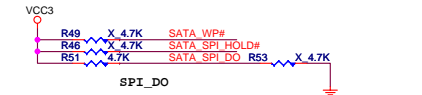
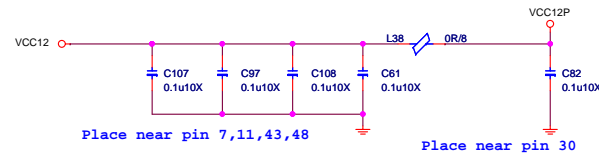
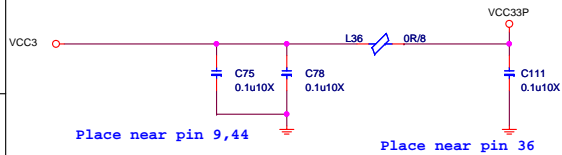


ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

330 mA

1,25V



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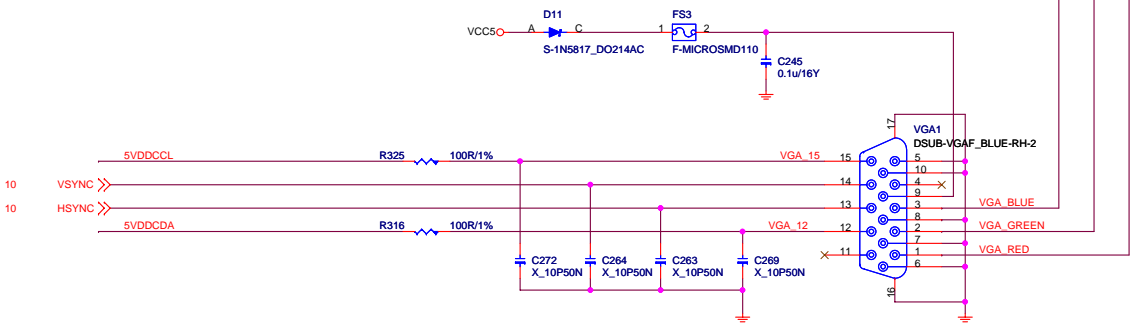
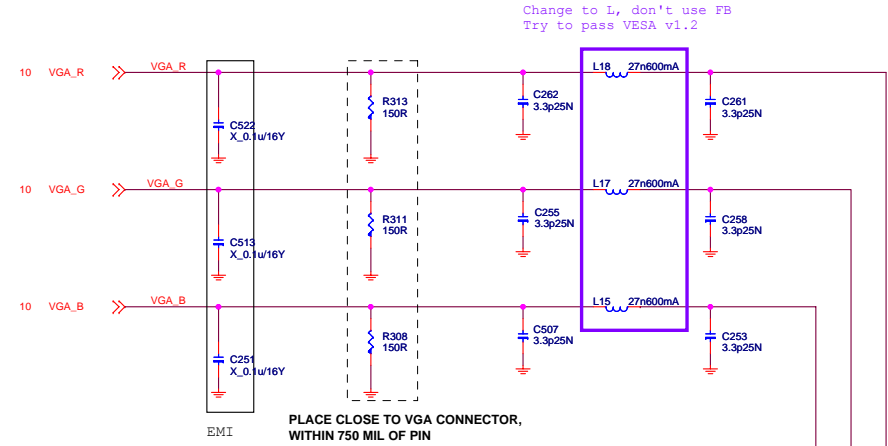
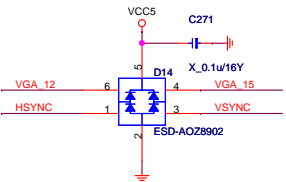
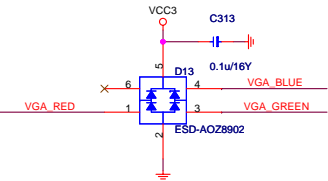
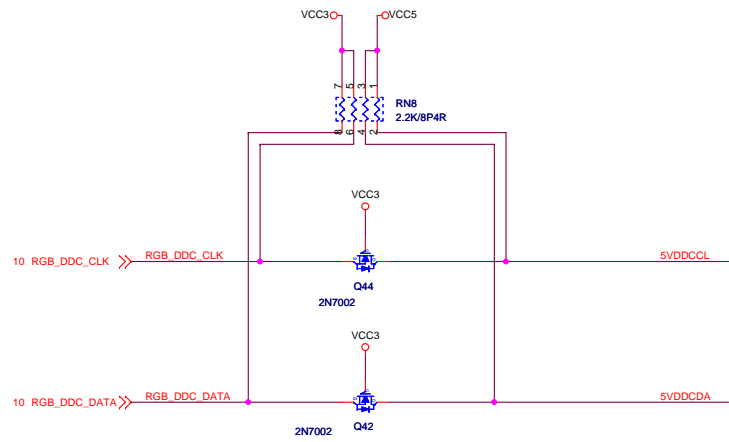
MS-7680

Size	Document Description	Rev
Custom	ASM1061 SATA6G	3.1
Date: Thursday, December 30, 2010	Sheet 21 of 39	

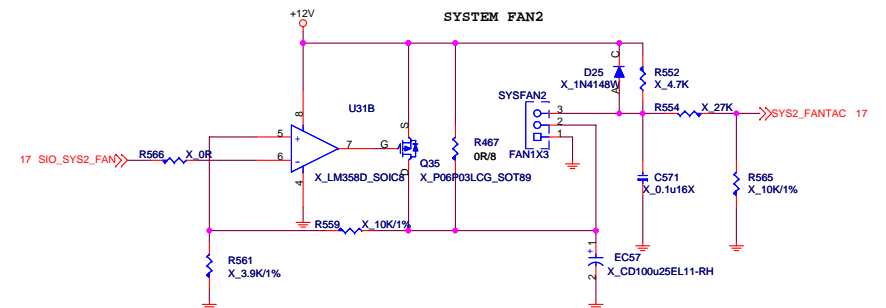
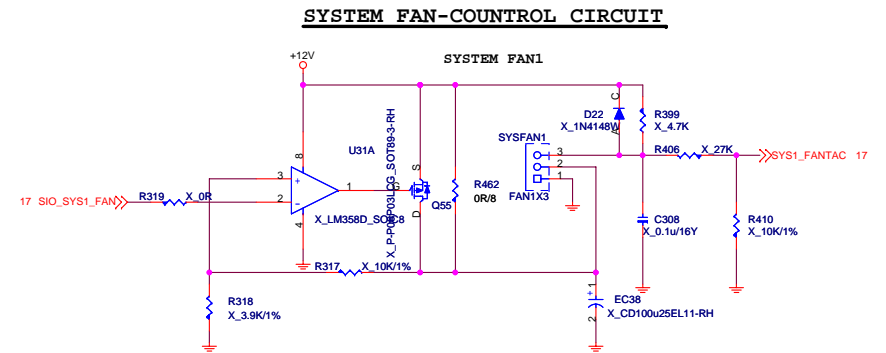
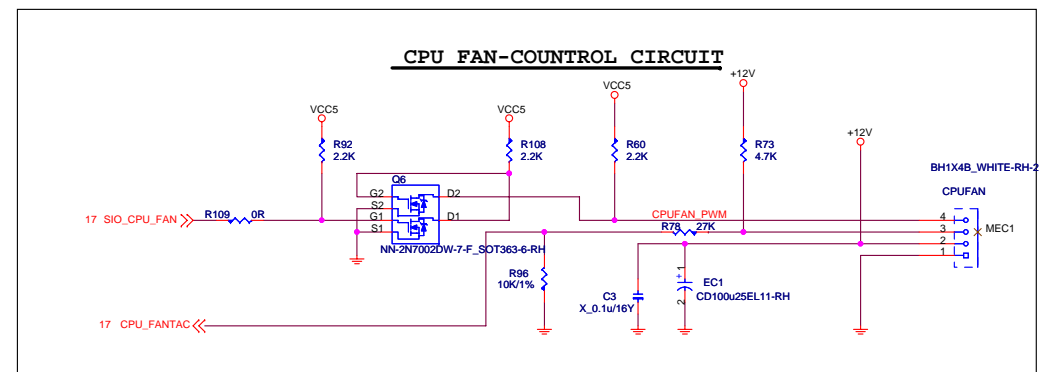
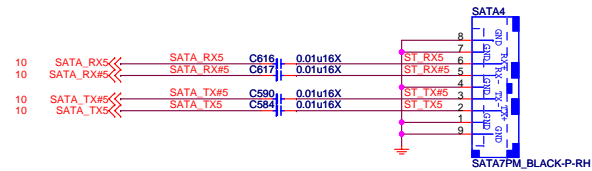
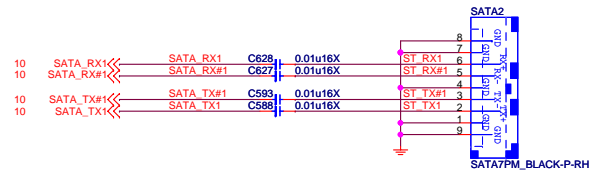
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



H61 PORT 0/1 3G
H67 PORT 0/1 6G

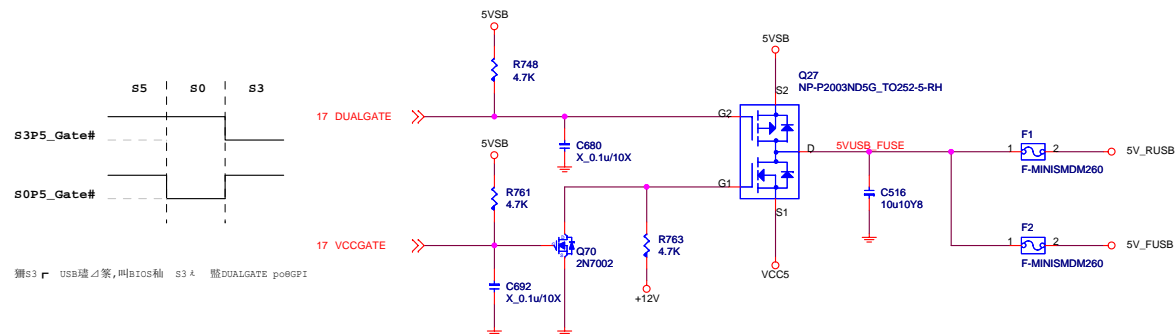


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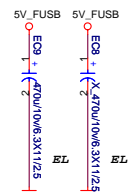
MS-7680

Size Custom	Document Description SATA / FAN Control	Rev 3.1
Date: Tuesday, January 04, 2011		Sheet 26 of 39

5V_RUSB Switch

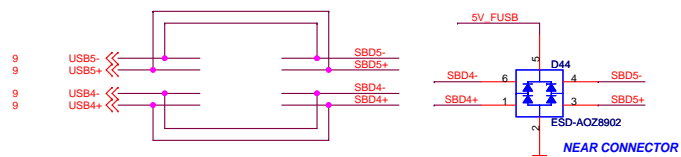


Front USB Connector

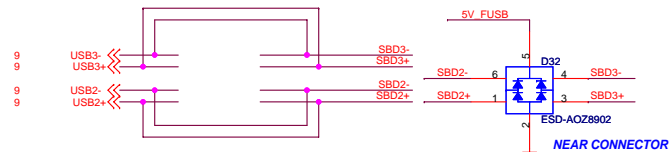


For H61 6,7,12,13 Port should be remove

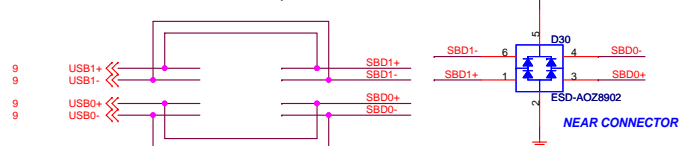
FRONT USB PORT 4,5



FRONT USB PORT 2,3

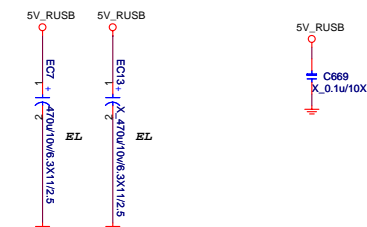


FRONT USB PORT 0,1

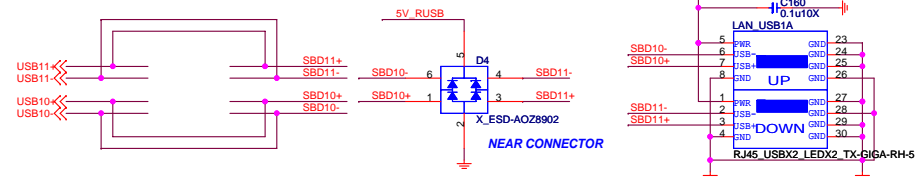


Rear USB Connector

NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)

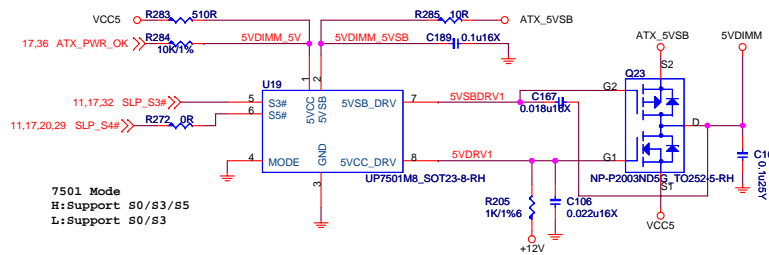


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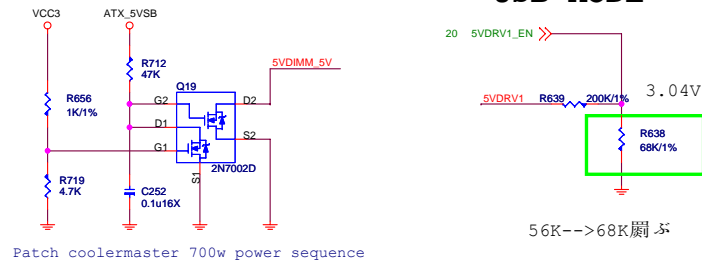
MS-7680

Size Custom	Document Description USB Connector	Rev 3.1
Date: Thursday, December 30, 2010		Sheet 27 of 39

5VDIMM FOR DDR

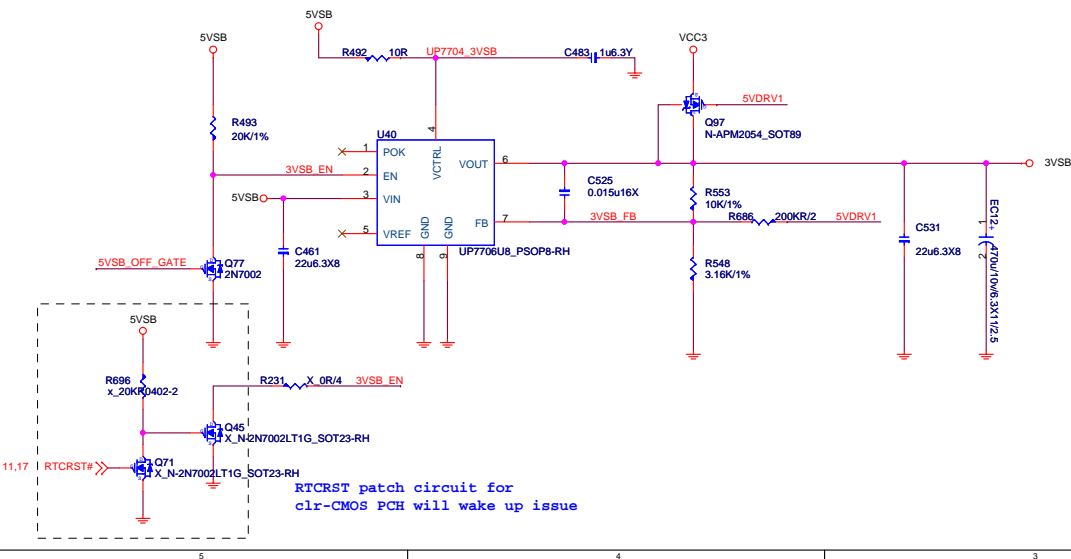


USB MODE

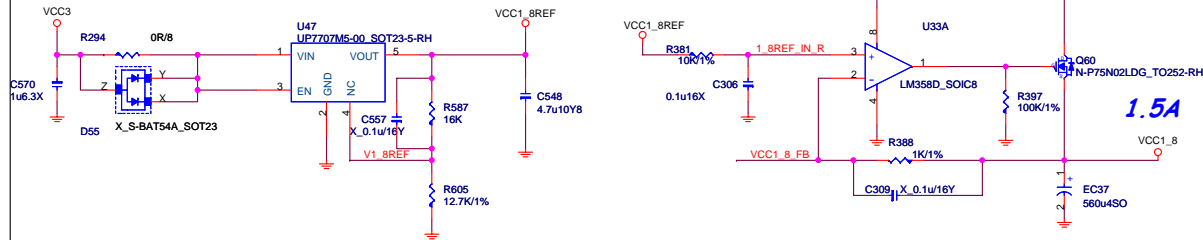


3VSB

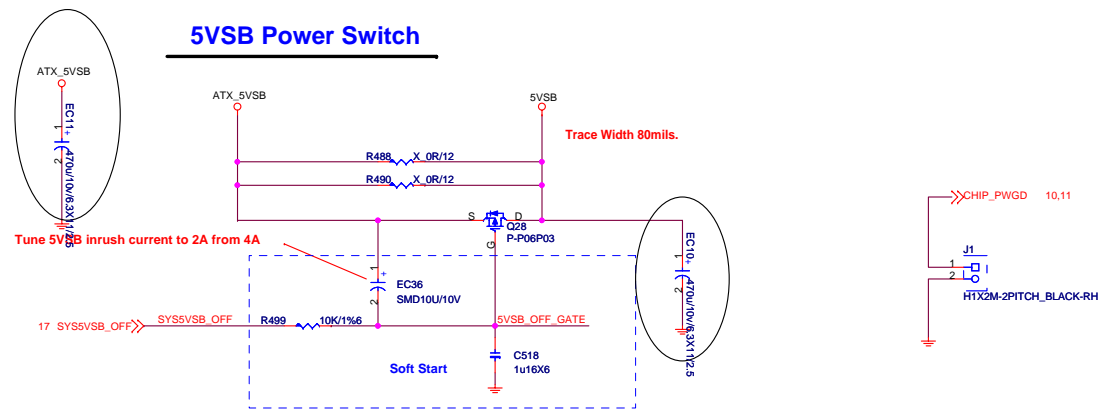
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



VCC1_8REF



5VSB Power Switch

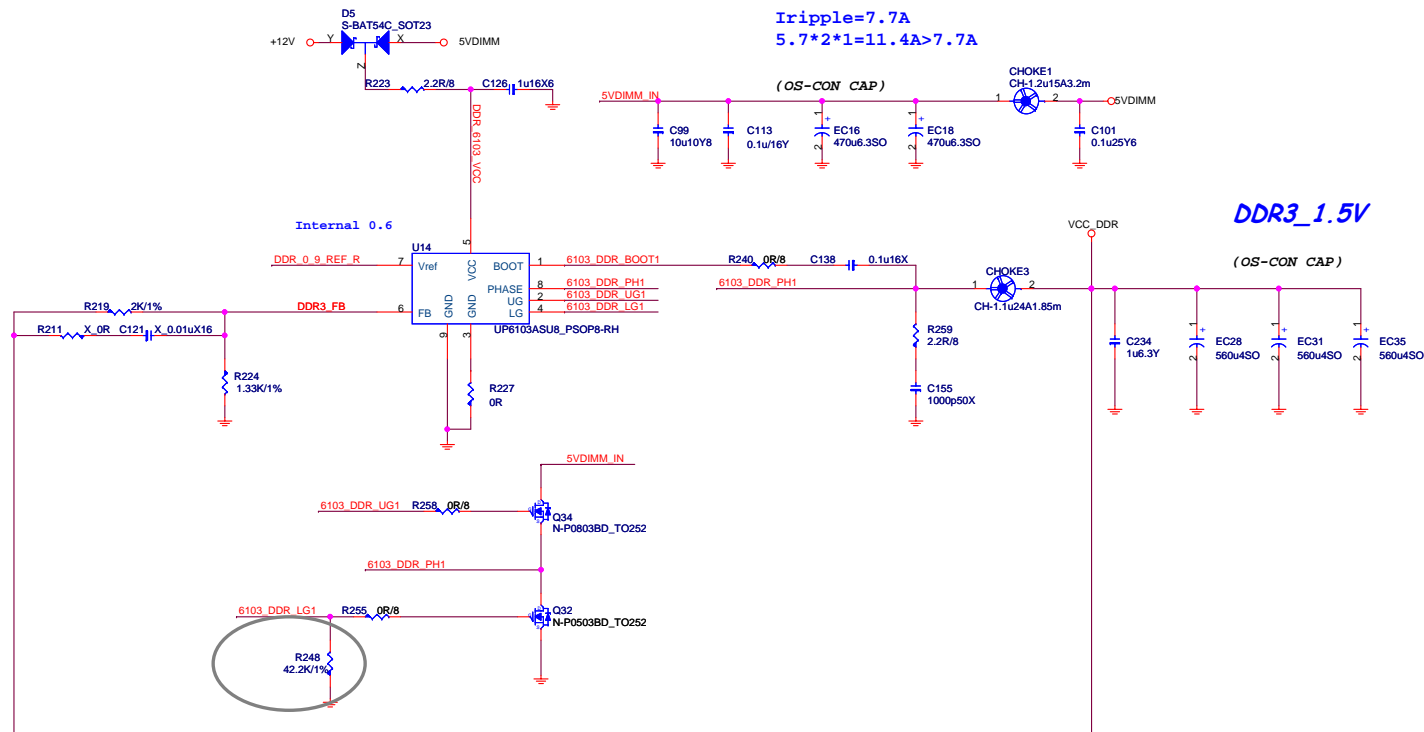
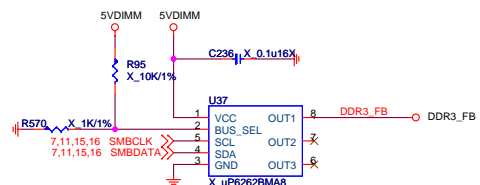
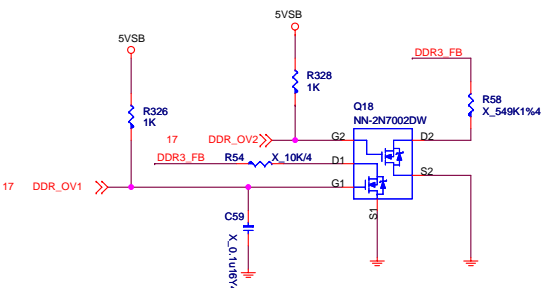


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MS-7680

Size Custom	Document Description ACPI controller UPI	Rev 3.1
Date: Tuesday, January 04, 2011		Sheet 28 of 39

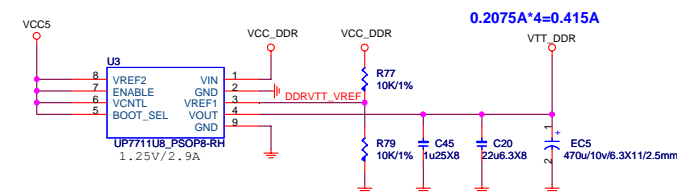
4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT



0x20:RH=10K,RL=OPEN

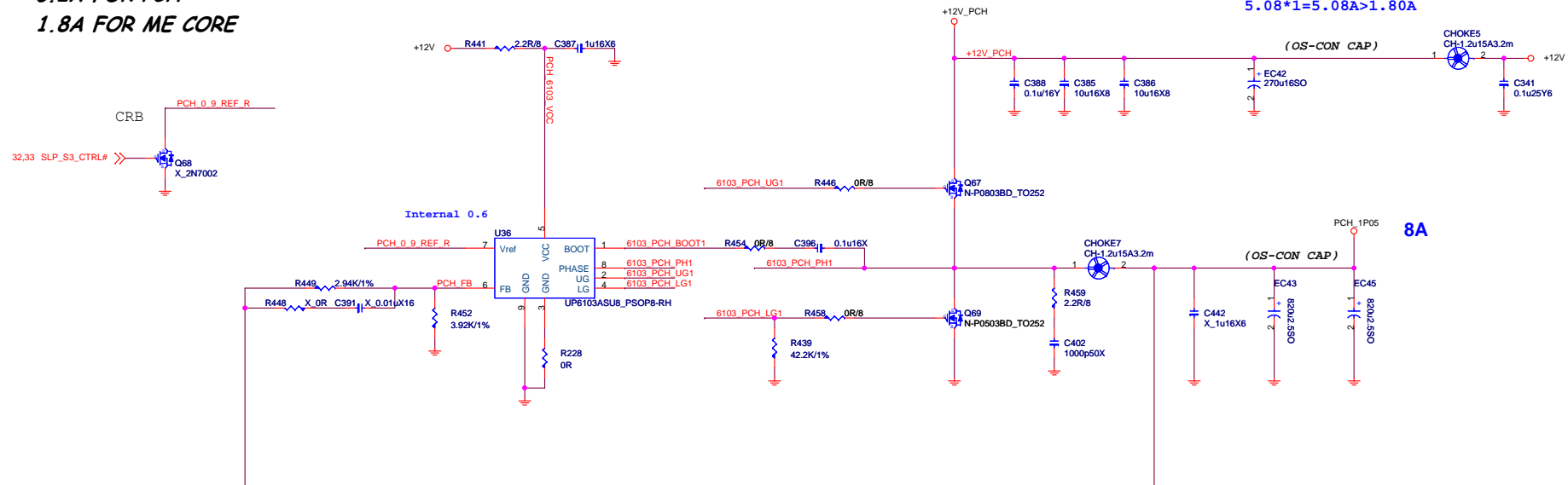
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

**MS-7680**

Size Custom	Document Description DDR Power - uP6103 1-Phase	Rev 3.1
Date: Thursdav. December 30, 2010		Sheet 29 of 39

1.8A FOR ME CORE

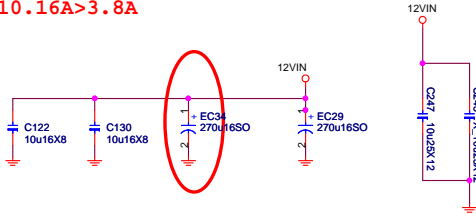
**MS-7680**

Size Custom	Document Description PCH Power - uP6103 1-Phase	Rev 3.1
Date: Thursday, December 30, 2010		Sheet 30 of 39

CPU_VTT:1.05/1.00

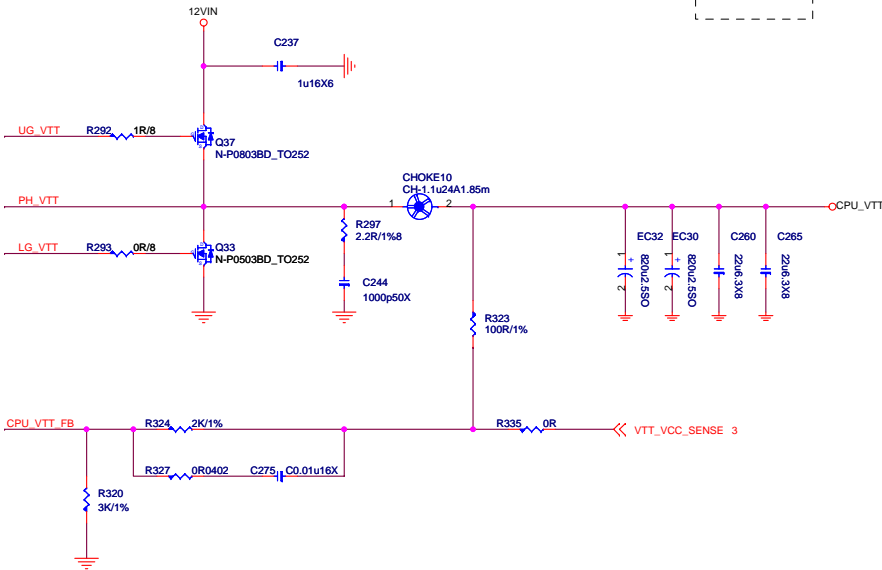
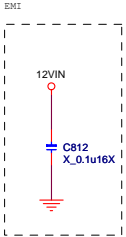
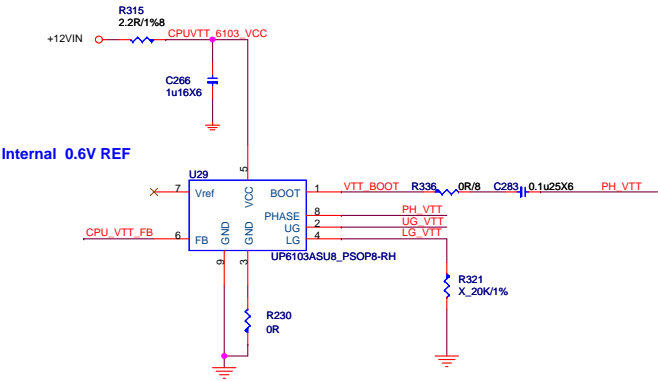
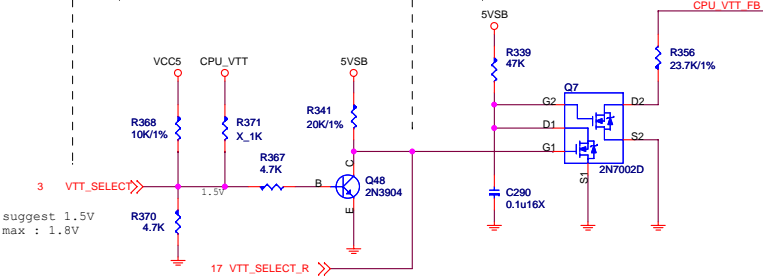
CPU VTT 8.5A + SA Core =8.8A =17.3A

Iripple=1.92(vtt)+1.88(sa)
5.08*2=10.16A>3.8A



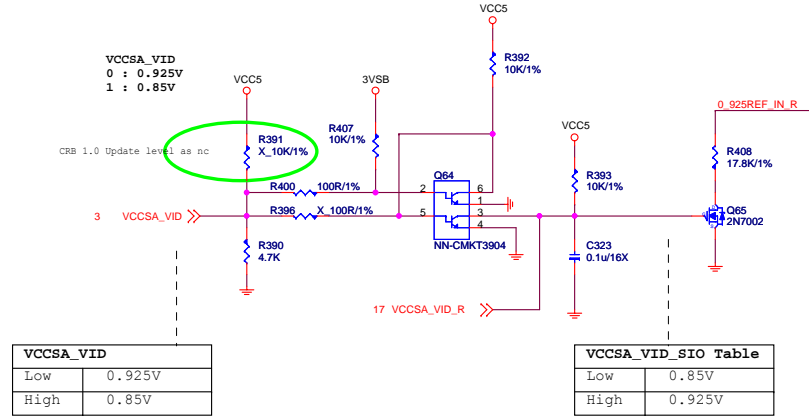
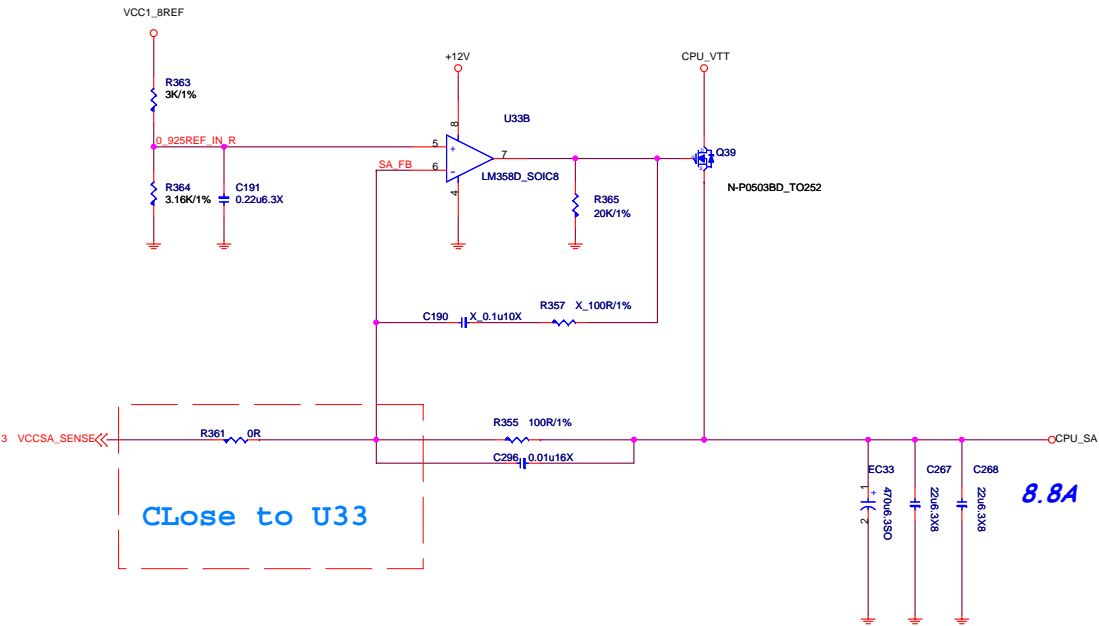
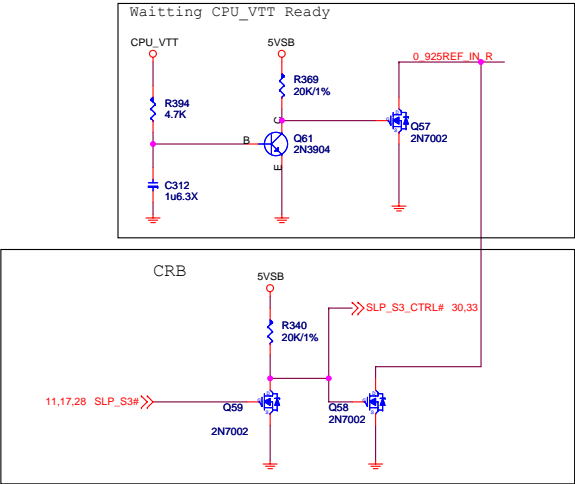
VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



CPU_SA:0.925/0.85

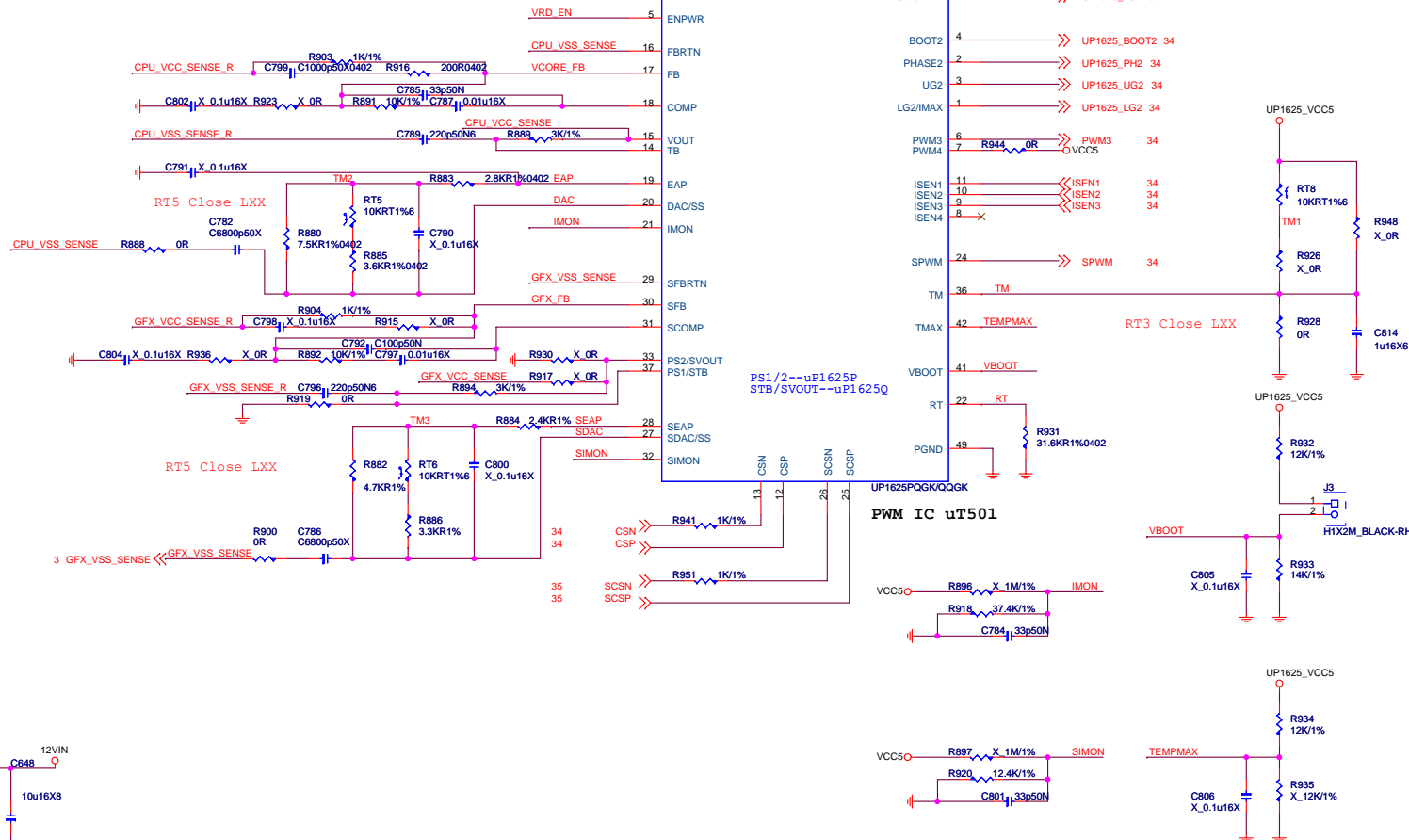
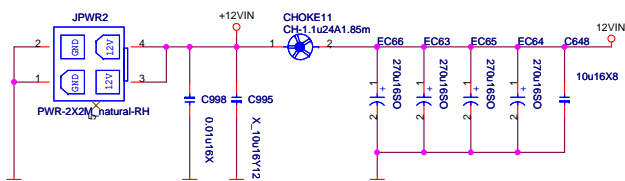
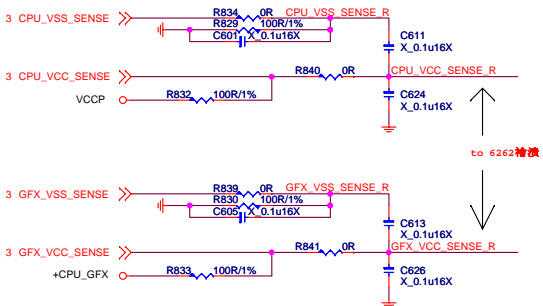
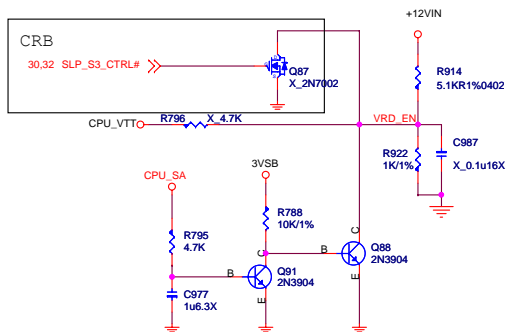
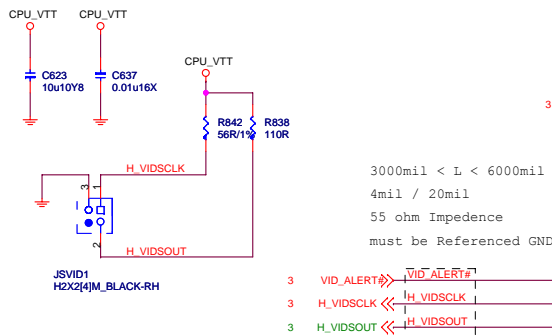
SA Core =8.8A



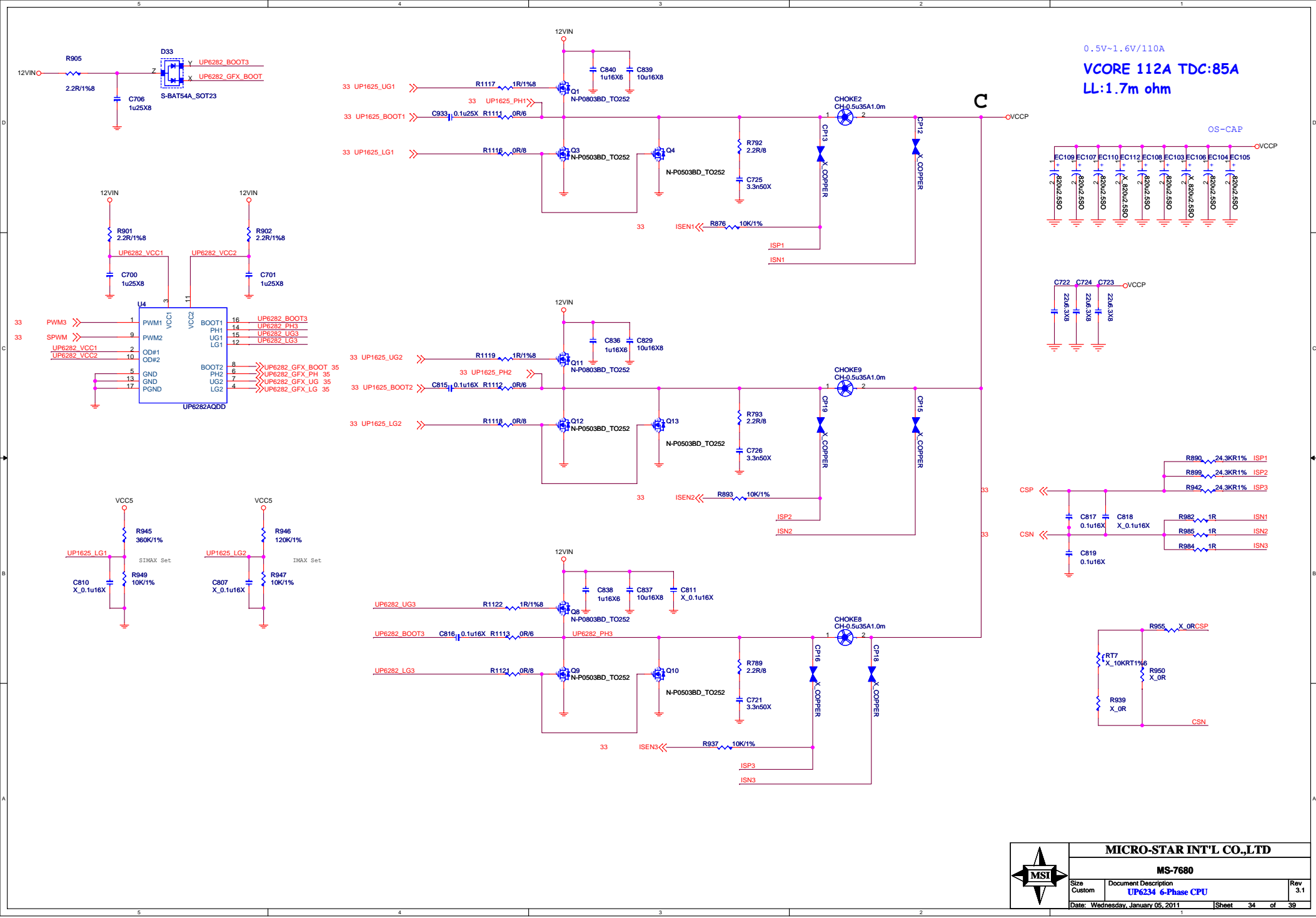
VCCSA_VID	
Low	0.925V
High	0.85V

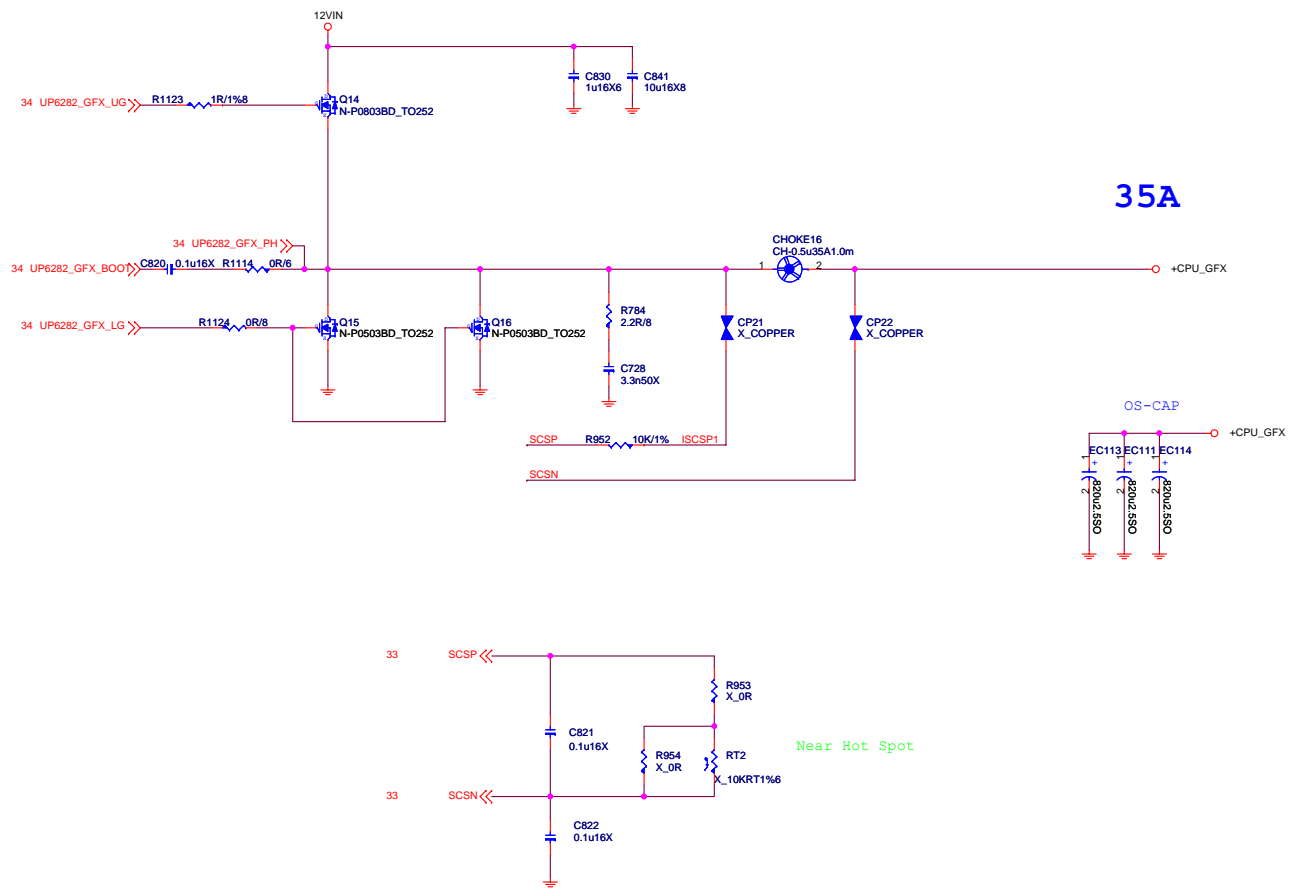
VCCSA_VID_SIO Table	
Low	0.85V
High	0.925V



Rev
3.

Date: Wednesday, January 05, 2011 Sheet 33 of 39





35A

Near Hot Spot

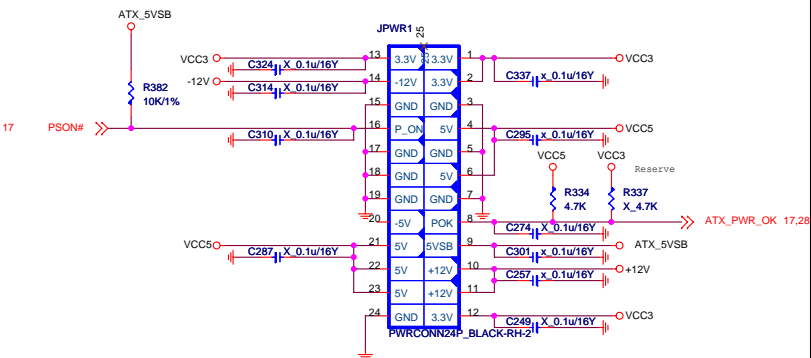


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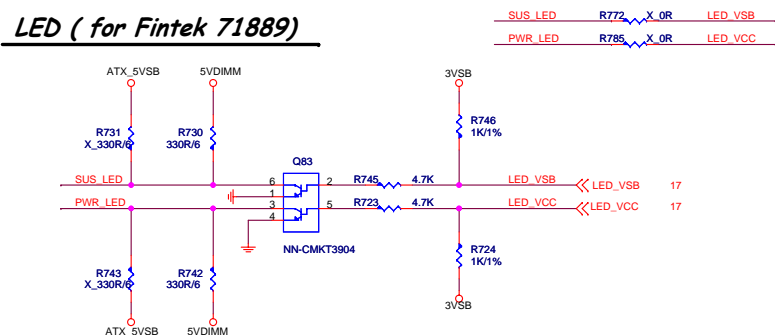
MS-7680

Size Custom	Document Description UP6234 1-Phase GPU	Rev 3.1
Date: Thursday, December 30, 2010	Sheet 35 of 39	

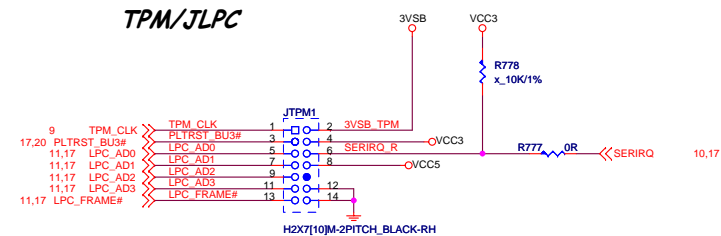
ATX POWER CONNECTOR



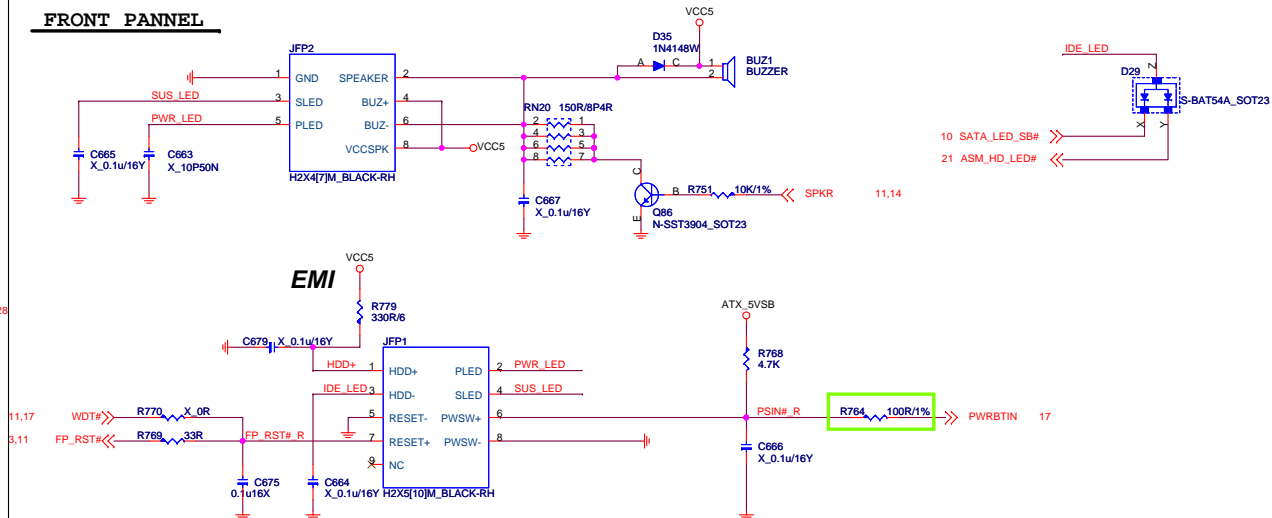
LED (for Fintek 71889)



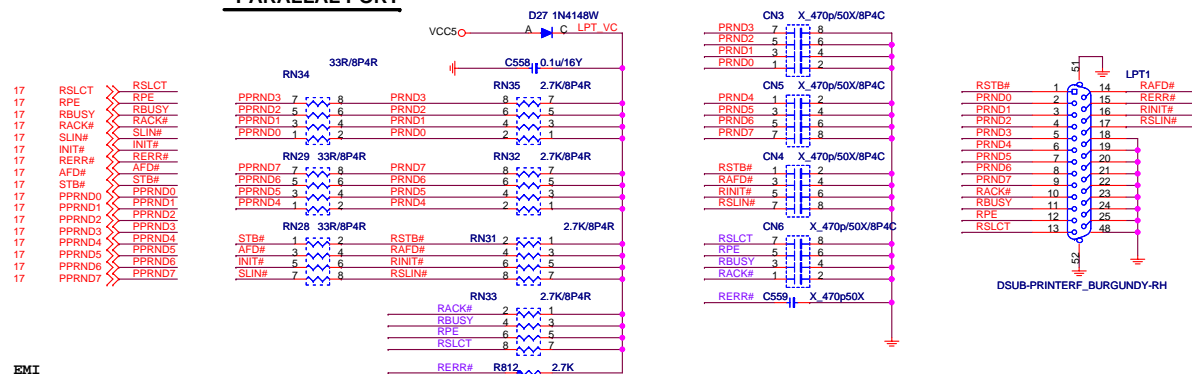
TPM/JLPC



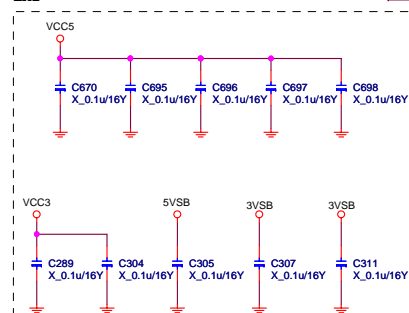
FRONT PANNEL



PARALLAL PORT



EMI



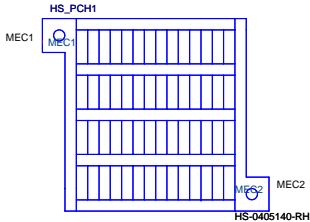
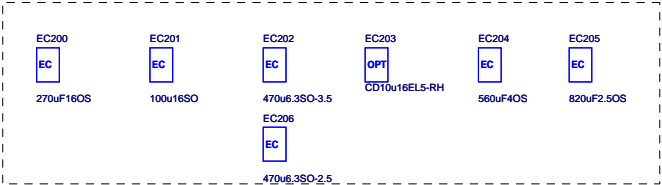
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MS-7680

Size Custom	Document Description ATX PWR-Connector & Front Panel & EMI	Rev 3.1
Date: Thursday, December 30, 2010		Sheet 36 of 39

PCH XDP PWRGD/RESET

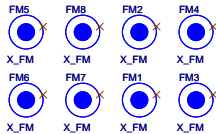
EL/OS OPT.



Simulation



Optical Fiducial Marks-120



Mounting Holes

